# User's Manual

## SAPPHIRE EDGE+ VPR-7X100-SYS
## RAVE2-MAX SYSTEM

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These specifications are subject to change without notice.

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November 13, 2026

## Federal Communications Commission (FCC) Statement

This device has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with instructions contained in this manual, may cause harmful interference to radio and television communications. However, there is no guarantee that interference will not occur in a particular installation.

If this product does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the product into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Note1: Connecting this device to peripheral devices that do not comply with Class B requirements, or using an unshielded peripheral data cable, could also result in harmful interference to radio or television reception.

Note2: The user is cautioned that any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this product.

Note3: To ensure that the use of this product does not contribute to interference, it is necessary to use shielded I/O cables.

## CE: Radiation of EN 55032 & Immunity of EN 55035

## Waste Electrical and Electronic Equipment (WEEE) Statement

To protect the global environment, this product must be sent to separate collection facilities for recovery and recycling.



**DISPOSAL**

Do not dispose of this product as unsorted municipal waste. Collect such waste separately for special treatment.

## Manufacturer

Sapphire Technology Pte. Ltd.

350 Orchard Road, Shaw House, #11-08, Singapore 238868

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# Chapter 1 Introduction

## *1.1 Package Contents*

Your RAVE2-MAX system comes with the following items.

- ☑ 1 x RAVE2-MAX system
- ☑ 5 x MINI DP(M) TO DP(F) Cables
- ☑ 1 x 12V/240W Power Adapter
- ☑ 1 x North American Power Cord (NA-C13)

If any items are missing or appear damaged, contact your authorized dealer.




<< RAVE2-MAX System Picture >>

## *1.2 Product Feature and Specifications*

### Product Features

- The RAVE2-MAX combines next generation of AMD Ryzen™ AI Embedded X100 Series processors with the latest AMD Versal™ AI Edge Series Gen 2 adaptive SoC devices on a single heterogeneous compute platform.

- The RAVE2-MAX features a sleek and compact red-and-black design in a Flex-ATX form factor. The RAVE2-MAX is well suited for more demanding AI applications in automotive and autonomous systems.

- Available as either a complete embedded system or Flex-ATX platform, RAVE2-MAX is purpose built for autonomous applications including advanced driver-assistance systems (ADAS), autonomous vehicles, robotaxis, autonomous mobile robots and off-highway commercial vehicles.

  With 12 GMSL2 camera ports and dual CAN Bus interfaces, it provides the connectivity needed for surround-camera perception and in-vehicle networking straight out of the box.

- The RAVE2-MAX Flex-ATX embedded motherboard is a powerful combination of AMD Ryzen™ AI Embedded X100 Series APU (Zen 5 CPU, RDNA 3.5 GPU, 50+ TOPS XDNA2 NPU) with AMD Versal™ AI Edge Series Gen2 2VE3558 adaptive SoC (world class programmable logic, ARM CPUs, AI engines).

  Supports quad 4K displays, 10GbE, M.2 WIFI, M.2 SSD storage, and USB interfaces to offload the Versal adaptive SoC of non-time critical functions. The Versal adaptive SoC is dedicated to real time preprocessing, sensor ingress, AI inference and low-latency adaptive processing tasks.

- Optional plugin expansion boards are available to support a variety of sensor interfaces.

  Versal adaptive SoC's programmable I/O allows for connection to many sensor interfaces, as well as the ability to scale for future interface requirements.

  - GMSL2 + CAN + miniDP + PMOD Header (GPIOx8)

## Product Specifications

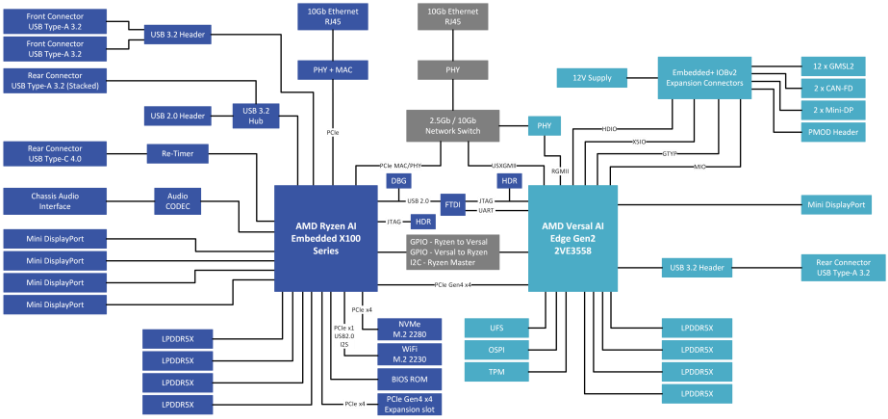
This RAVE2-MAX system consists of RAVE2-MAX motherboard and AUTO I/O board .

| RAVE2-MAX motherboard | |
|---|---|
| **AMD Embedded+ Architecture** | AMD Ryzen™ AI Embedded X100 Series APU + AMD Versal™ AI Edge Series Gen2 2VE3558 SoC on single board |
| **Adaptive SoC Subsystem** | ◆ AMD Versal™ AI Edge Series Gen2 2VE3558 SoC<br>◆ Display : 1 x dedicated miniDP + 2 x miniDP from IO board<br>◆ UFS : 256G UFS3.1<br>◆ LPDDR Memory : 16GB LPDDR5x Memory (4x 4GB, 8533 MT/s)<br>◆ USB Type A : 1 x USB3.2 Gen2 Type A<br>◆ TPM : TPM 2.0 (Infineon OPTIGA™ TPM SLM 9672)<br>◆ OSPI : 1 Gb NOR-Flash for Local Boot<br>◆ EEPROM : 64 Kb for Board-ID<br>◆ LED : 1 x Done, 1 x ERROR_OUT, 1 x RPU_Status<br>◆ 10GbE : Shared with APU thru Ethernet switch<br>◆ PCIe : Gen4 x 2 (Dedicated for Processor Connection)<br>◆ IO Expansion Connector : 250 Pin Socket |
| **Processor** | AMD Ryzen™ AI Embedded X100 Series |
| **Processor Memory** | 128GB LPDDR5x Memory (8x 16GB, 8000 MT/s) |
| **External I/O Edge Connectors** | x86 Processor Subsystem<br>◆ Display : 4 x mini DP<br>◆ Ethernet : 1 x 10GbE port dedicated to APU<br>1 x 10GbE port available for APU 10GbE, APU 1GbE and 10GbE Versal through Ethernet switch<br>◆ USB Type A : 2 x USB3.2 Gen2 Type A<br>◆ USB Type C : 1 x USB4.0 Type C |
| **Internal I/O Headers** | x86 Processor Subsystem<br>◆ Front Panel : 5x2pins (power button)<br>◆ Audio : 2x5pin (1 x Line-Out, 1 x Mic-In)<br>◆ USB : 1 x USB3.2 / 2.0 (2x10pin) & 1 x USB2.0 (2x5pin)<br>◆ OcuLink PCIe Gen4 x4<br>◆ USB Type C Connector (USB3-DEBUG) |
| **Expansion IO Slots** | ◆ 1 x M.2 Key M 2280 for 1TB SSD (PCIe Gen4 x4)<br>◆ 1 x M.2 Key E 2230 for Wireless/BT (PCIe Gen4 x1,I2S and USB2.0) |

| | |
|---|---|
| **OS** | Ubuntu 22.04 |
| **Cooler Type** | Active |
| **Power Input** | DC 12V 240W Jack |
| **Form Factor** | Chassis (W x D x H) : 220 x 283 x 60 mm<br>Motherboard : Flex-ATX, 229 x 191 mm (9.0" x 7.5") |
| **Operating Temperature Range** | Ambient 0°C to 60°C |

| **AUTO I/O board** | |
|---|---|
| **IO Expansion Board** | ◆ 3 x GMSL2,<br>◆ 2 x CAN-FD,<br>◆ 2 x miniDP,<br>◆ 1 x PMOD Header (GPIOx8) |

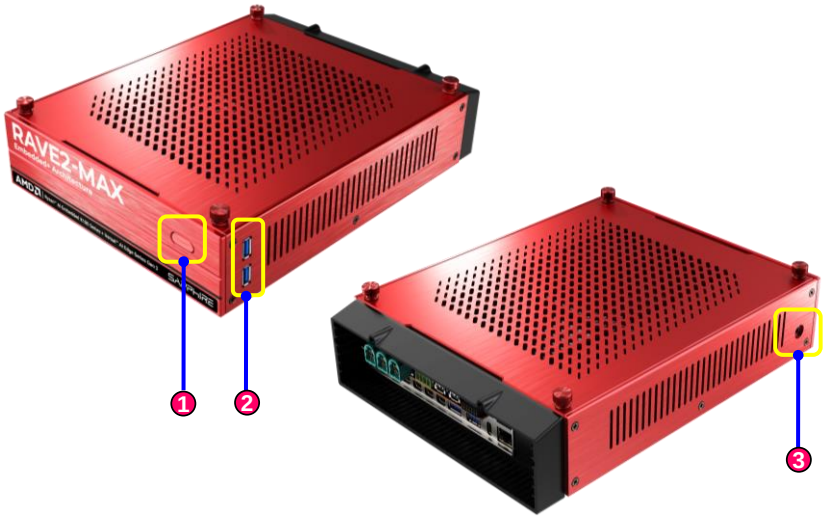
# *1.3 Block Diagram of motherboard*



# Chapter 2 Product Overview

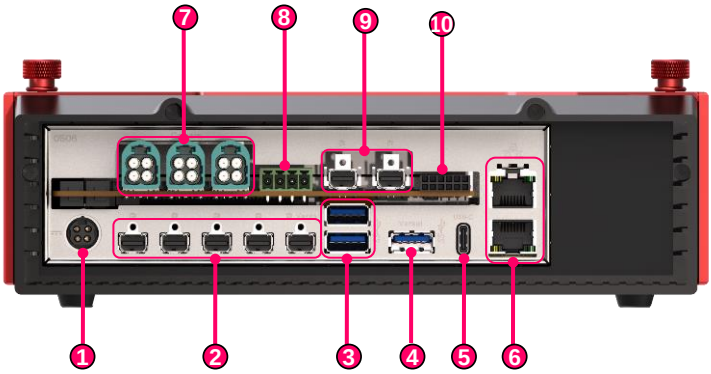
This chapter shows the location of components and description on the RAVE2-MAX system.

## *2.1 Front and Side View of Product*



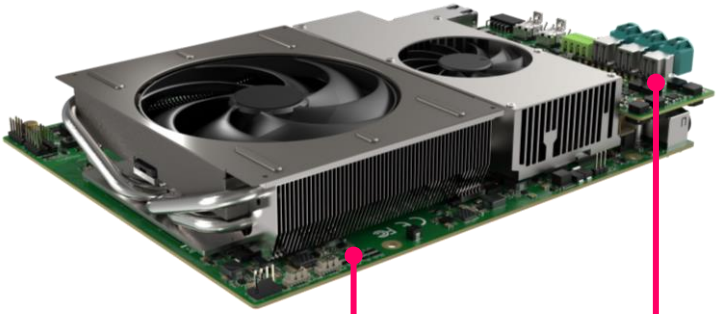

| Item | Description |
|---|---|
| 1 | POWER On/Off button |
| 2 | USB3.2 Gen 2 Type A Port*2 |
| 3 | Audio Port |

## 2.2 Rear View of Product




| Item | Description |
|---|---|
| From RAVE2-MAX motherboard | |
| 1 | DC-IN 12V 240W Jack |
| 2 | Mini Display Port *5 |
| 3 | USB3.2 Gen 2 Type A Port *2 |
| 4 | USB3.2 Gen 2 Type A Port *1 (from 2VE3558) |
| 5 | USB4 Type C Port |
| 6 | 10G bps RJ45 LAN Port *2 |
| From AUTO I/O board | |
| 7 | FAKRA connector *3 |
| 8 | CAN connector |
| 9 | Mini Display Port *2 |
| 10 | PMOD connector |

## *2.3 Inside View of Product*



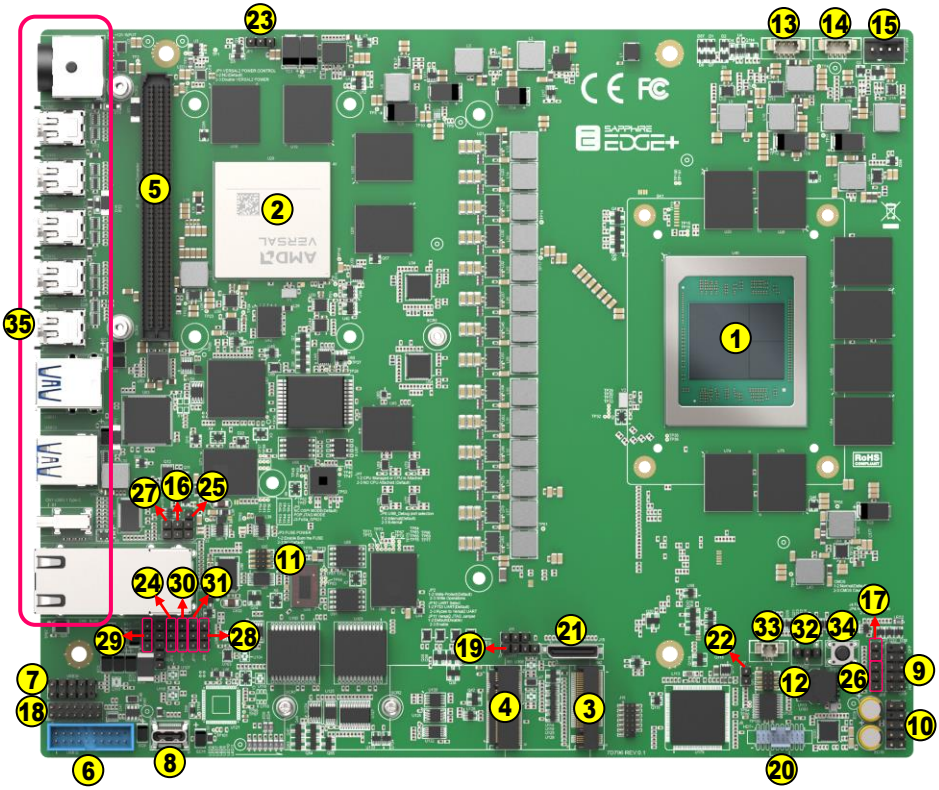
**AUTO I/O Board**

**RAVE2-MAX Motherboard**

# Chapter 3 Motherboard and I/O Board

## *3.1 Motherboard Layout*

The following figure shows the location of components and description on the motherboard . See next page for component description.

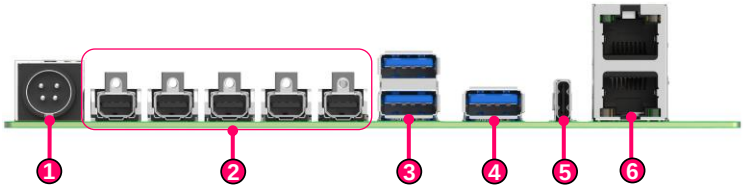



Note:
Picture is for reference only, actual board may be slightly different.

| Item | Component description | Location |
|---|---|---|
| 1 | AMD Ryzen™ AI Embedded X100 Series Processor | U46 |
| 2 | AMD Versal AI Edge Gen2 2VE3558 IC | U28 |
| 3 | M.2 M-key 2280 slot for SSD device | M2 |
| 4 | M.2 E-Key 2230 slot for Wifi/BT board | M1 |
| 5 | I/O Expansion Board Socket | J2 |
| 6 | USB3.2 Gen2 Header (Note), 2x10pin 2.00mm pitch | USB32 |
| 7 | USB 2.0 Header (Note), 2x5pin 2.54mm pitch | USB34 |
| 8 | Internal USB INPUT connector for 2VE3558 debug use | USB3-DEBUG |
| 9 | Front Panel Header, 2x5pin 2.54mm pitch | CFP |
| 10 | Front Panel Audio, 2x5pin 2.54mm pitch | CFPA |
| 11 | I2C Header, 2x4pin 1.27mm pitch | I2C |
| 12 | SPI Header, 2x4pin 1.27mm pitch | SPI |
| 13 | MIO Fan Header, 1x4pin 1.25mm pitch | MIOFAN |
| 14 | CPU Fan Header, 1x4pin 1.25mm pitch | CPUFAN |
| 15 | SYSTEM Fan Header, 1x4pin 2.54mm pitch | SYSFAN |
| 16 | 2VE3558 GPIO1 Header, 1x2pin 2.54mm pitch | J3 |
| 17 | 2VE3558 GPIO2 Header, 1x2pin 2.54mm pitch | J4 |
| 18 | AMD FPGA JTAG Port, 2x7pin 2.0mm pitch | J5 |
| 19 | UART Header, 1x4pin 2.54mm pitch | J7 |
| 20 | AMD APU HDT+ Header, 2x10pin 1.27mm pitch | J8 |
| 21 | OCULINKX4 Connector, 42pin | J15 |
| 22 | Case Open Header, 1x2pin 2.54mm pitch | J17 |
| 23 | VERSAL2 Power Control Jumper, 1x3pin 2.54mm pitch | JP1 |
| 24 | ROM Write Protect mode Jumper, 1x3pin 2.54mm pitch | JP2 |
| 25 | FUSE Power Control Jumper, 1x3pin 2.54mm pitch | JP3 |
| 26 | Auto Power ON Jumper, 1x3pin 2.54mm pitch | JP4 |
| 27 | 2VE3558 MODE Selection, 1x2pin 2.54mm pitch | JP5 |
| 28 | USB Debug Port Selection Jumper of 2VE3558, 1x3pin 2.54mm pitch | JP6 |
| 29 | MDIO Select Jumper, 1x3pin 2.54mm pitch | JP7 |
| 30 | UART Select Jumper, 1x3pin 2.54mm pitch | JP10 |
| 31 | Versal2 JTAG Jumper, 1x3pin 2.54mm pitch | JP11 |
| 32 | Clear CMOS Jumper, 1x3pin 2.54mm pitch | CMOS |
| 33 | Battery headers, 1x2pin 1.25mm pitch | BAT |
| 34 | 2VE3558 Reset button | SW1 |
| 35 | Back Panel Connectors (see next page for detail) | |

Note: Each USB 3.2 / USB2.0 Header can be used to connect 2 USB devices.

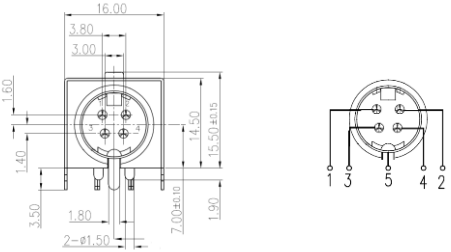
## I/O Back Panel



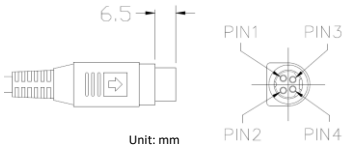

| Item | Description | Item | Description |
|---|---|---|---|
| 1 | DC-IN 12V 240W Jack | 4 | USB3.2 Gen 2 Type A Port *1 (from 2VE3558) |
| 2 | Mini Display Port *5 | 5 | USB4 Type C Port |
| 3 | USB3.2 Gen 2 Type A Port *2 | 6 | 10G bps RJ45 LAN Port *2 |

### 1. DC-IN Jack (CN3)

The DC-IN Jack supports only 12V 240W Input.

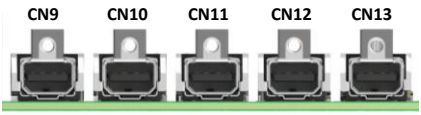


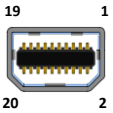

Reference DC power adapter: 12V 240W (FSP270-RHAN3)



## 2. Mini DisplayPort (five, CN9 to CN13)

The motherboard provides five Mini DisplayPort support for high resolution displays, digital content protection. With a suitable adapter, DisplayPort may be used to drive displays with a VGA, DVI or HDMI interface.



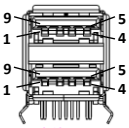




| CN9/CN10/CN11/CN12 from APU | | | |
|---|---|---|---|
| **Pin** | **Definition** | **Pin** | **Definition** |
| 1 | GND | 2 | Hot Plug Detect |
| 3 | ML_Lane 0 (p) | 4 | CONFIG1 |
| 5 | ML_Lane 0 (n) | 6 | CONFIG2 |
| 7 | GND | 8 | GND |
| 9 | ML_Lane 1 (p) | 10 | ML_Lane 3 (p) |
| 11 | ML_Lane 1 (n) | 12 | ML_Lane 3 (n) |
| 13 | GND | 14 | GND |
| 15 | ML_Lane 2 (p) | 16 | AUX_CH(p) |
| 17 | ML_Lane 2 (n) | 18 | AUX_CH(n) |
| 19 | GND | 20 | DP_PWR |

| CN13 from 2VE3558 | | | |
|---|---|---|---|
| **Pin** | **Definition** | **Pin** | **Definition** |
| 1 | GND | 2 | Hot Plug Detect |
| 3 | ML_Lane 0 (p) | 4 | CONFIG1 |
| 5 | ML_Lane 0 (n) | 6 | CONFIG2 |
| 7 | GND | 8 | GND |
| 9 | ML_Lane 1 (p) | 10 | NC |
| 11 | ML_Lane 1 (n) | 12 | NC |
| 13 | GND | 14 | GND |
| 15 | NC | 16 | AUX_CH(p) |
| 17 | NC | 18 | AUX_CH(n) |
| 19 | GND | 20 | DP_PWR |

### 3. USB3.2 Gen2 port (Dual, USB31)

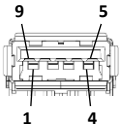
The motherboard provides one stacked USB3.2 Gen2 ports are backward compatible with USB 3.x/2.0 devices. Supports data transfer rates up to 10Gbps.




| Pin | Definition | Pin | Definition |
|---|---|---|---|
| 1 | +5V | 6 | SSTX+ |
| 2 | Data- | 7 | GND |
| 3 | Data+ | 8 | SSRX- |
| 4 | GND | 9 | SSRX+ |
| 5 | SSTX- | | |

### 4. USB3.2 Gen2 port (Single, USB33), from 2VE3558

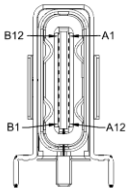
The motherboard provides one single USB3.2 Gen2 ports from 2VE3558 is backward compatible with USB 3.x/2.0 devices. Supports data transfer rates up to 10Gbps.




| Pin | Definition | Pin | Definition |
|---|---|---|---|
| 1 | +5V | 6 | SSTX+ |
| 2 | Data- | 7 | GND |
| 3 | Data+ | 8 | SSRX- |
| 4 | GND | 9 | SSRX+ |
| 5 | SSTX- | | |

### 5. USB4 Type C port (CN1)

The motherboard provides one USB4 Type C port are backward compatible with USB 3.x/2.0 devices. Supports data transfer rates up to 40Gbps.

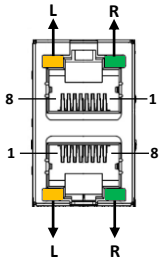



| Pin | Definition | Pin | Definition |
|---|---|---|---|
| A1 | GND | B1 | GND |
| A2 | DP_TX2P | B2 | DP_TX1P |
| A3 | DP_TX2N | B3 | DP_TX1N |
| A4 | POWER (+12V) | B4 | POWER(+12V) |
| A5 | DP_HPD | B5 | NC |
| A6 | NC | B6 | NC |
| A7 | NC | B7 | NC |
| A8 | DP_AUXP | B8 | DP_AUXN |
| A9 | POWER (+12V) | B9 | POWER(+12V) |
| A10 | DP_TX0N | B10 | DP_TX3N |
| A11 | DP_TX0P | B11 | DP_TX3P |
| A12 | GND | B12 | GND |

## 6. 10G bps RJ45 LAN Port (Dual, CN5)

The motherboard provides two 10G bps RJ-45 jacks for connecting to Local Area Network (LAN). Two LEDs are built into the RJ-45 LAN connector. These LEDs indicate the status of the LAN.

Upper LAN: from CUX3610




Lower LAN: from AQC113

| Pin | Definition | Pin | Definition |
|---|---|---|---|
| 1 | BI_DA+ | 5 | BI_DC- |
| 2 | BI_DA- | 6 | BI_DB- |
| 3 | BI_DB+ | 7 | BI_DD+ |
| 4 | BI_DC+ | 8 | BI_DD- |

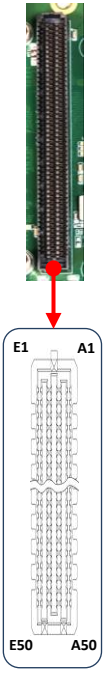
| LED | LED Color | LED state | Indicates |
|---|---|---|---|
| R | Green | Off | LAN link is not established |
| | | On | LAN link is established |
| | | Blinking | LAN activity is occurring |
| L | N/A | Off | 10M bps data rate |
| | Green | On | 100M/1G/2.5G/5G bps data rate |
| | Orange | On | 10G bps data rate |

# *3.2 Onboard Connector and Jumper*

## I/O Expansion Board Socket (J2)

The motherboard provides one I/O Expansion Board Socket, can be used to connect to an automotive I/O daughter board .

J2: I/O Expansion Board Socket (Manufacturer PN: SEAF-50-07.5-L-05-2-A-K-TR)

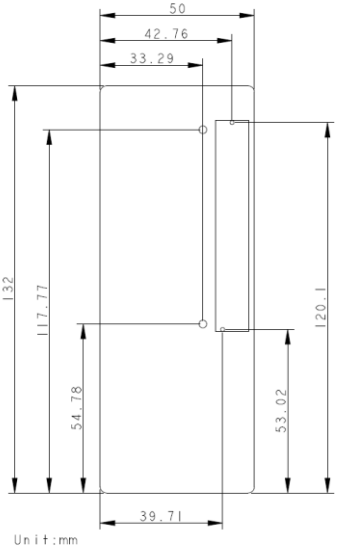



**I/O Expansion Board Socket Pin Definition**

| Pin# | Row A | Row B | Row C | Row D | Row E |
|---|---|---|---|---|---|
| 1 | CNCTR_12V | CNCTR_12V | CNCTR_12V | CNCTR_12V | CNCTR_12V |
| 2 | GND | GND | GND | GND | GND |
| 3 | PWR_EN | MIO_CAN0_WK | 1-Wire PROM | MIO_CAN1_WK | MIO_I2C_SCL |
| 4 | MIO_CAN0_TX | MIO_CAN0_RX | MIO_CAN1_TX | MIO_CAN1_RX | MIO_I2C_SDA |
| 5 | GND | GND | GND | GND | GND |
| 6 | GND | GND | GND | GND | GND |
| 7 | GTYP_TX0_P | GND | GTYP_REFCLK0_P | GND | GTYP_RX1_P |
| 8 | GTYP_TX0_N | GND | GTYP_REFCLK0_N | GND | GTYP_RX1_N |
| 9 | GND | GTYP_TX2_P | GND | GTYP_RX0_P | GND |
| 10 | GND | GTYP_TX2_N | GND | GTYP_RX0_N | GND |
| 11 | GTYP_TX1_P | GND | GTYP_REFCLK1_P | GND | GTYP_RX2_P |
| 12 | GTYP_TX1_N | GND | GTYP_REFCLK1_N | GND | GTYP_RX2_N |
| 13 | GND | GTYP_TX3_P | GND | GTYP_RX3_P | GND |
| 14 | GND | GTYP_TX3_N | GND | GTYP_RX3_N | GND |
| 15 | GND | GND | GND | GND | GND |
| 16 | GND | GND | GND | GND | GND |
| 17 | O0.P0<br>TRIO0_A | O0.P2<br>TRIO0_C | O0.P4<br>TRIO1_C | O0.P6<br>TRIO1_A | O3.P0<br>TRIO6_A |
| 18 | O0.P1<br>TRIO0_B | O0.P3<br>GPIO | O0.P5<br>GPIO | O0.P7<br>TRIO1_B | O3.P1<br>TRIO6_B |
| 19 | GND | GND | GND | GND | GND |
| 20 | O1.P0<br>TRIO2_A | O1.P2<br>TRIO2_C | O1.P4<br>TRIO3_C | O1.P6<br>TRIO3_A | O3.P2<br>TRIO6_C |
| 21 | O1.P1<br>TRIO2_B | O1.P3<br>GPIO | O1.P5<br>GPIO | O1.P7<br>TRIO3_B | O3.P3<br>GPIO |
| 22 | GND | GND | GND | GND | GND |
| 23 | O2.P0<br>TRIO4_A | O2.P2<br>TRIO4_C | O2.P4<br>TRIO5_C | O2.P6<br>TRIO5_A | O3.P5<br>GPIO |
| 24 | O2.P1<br>TRIO4_B | O2.P3<br>GPIO | O2.P5<br>GPIO | O2.P7<br>TRIO5_B | O3.P4<br>TRIO7_C |
| 25 | GND | GND | GND | GND | GND |
| 26 | O0.P6<br>GC_P | X5IO1_VCCO<br>BANK709_VCCO | GND | X5IO0_VCCO<br>BANK708_VCCO | O3.P6<br>TRIO7_A |
| 27 | O0.P7<br>GC_N | X5IO1_VCCO<br>BANK709_VCCO | GND | X5IO0_VCCO<br>BANK708_VCCO | O3.P7<br>TRIO7_B |
| 28 | GND | GND | GND | GND | GND |
| 29 | O0.P0<br>DPHY_DATA_P | O0.P2<br>DPHY_CLK_P | O0.P4<br>DPHY_DATA_P | O3.P6 | O3.P4<br>DPHY_DATA_P |
| 30 | O0.P1<br>DPHY_DATA_N | O0.P3<br>DPHY_CLK_N | O0.P5<br>DPHY_DATA_N | O3.P7 | O3.P5<br>DPHY_DATA_N |
| 31 | GND | GND | GND | GND | GND |
| 32 | O1.P0<br>DPHY_DATA_P | O1.P2<br>DPHY_CLK_P | O1.P4<br>DPHY_DATA_P | O1.P6<br>DPHY_DATA_P | O3.P2<br>DPHY_CLK_P |
| 33 | O1.P1<br>DPHY_DATA_N | O1.P3<br>DPHY_CLK_N | O1.P5<br>DPHY_DATA_N | O1.P7<br>DPHY_DATA_N | O3.P3<br>DPHY_CLK_N |
| 34 | GND | GND | GND | GND | GND |

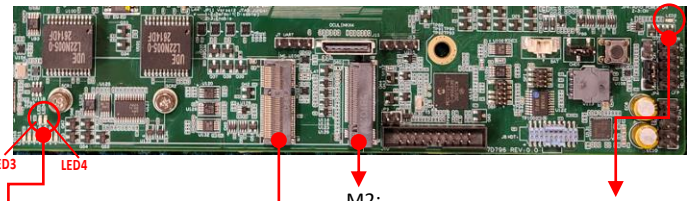
| | | | | | |
|---|---|---|---|---|---|
| 35 | O2.P0<br>DPHY_DATA_P | O2.P2<br>DPHY_CLK_P | O2.P4<br>DPHY_DATA_P | O2.P6<br>DPHY_DATA_P | O3.P0<br>DPHY_DATA_P |
| 36 | O2.P1<br>DPHY_DATA_N | O2.P3<br>DPHY_CLK_N | O2.P5<br>DPHY_DATA_N | O2.P7<br>DPHY_DATA_N | O3.P1<br>DPHY_DATA_N |
| 37 | GND | GND | GND | GND | GND |
| 38 | HDIO0_0 | HDIO0_1 | HDIO0_2 | HDIO0_3 | HDIO0_4 |
| 39 | HDIO0_5 | HDIO0_6 | HDIO0_7 | HDIO0_8 | HDIO0_9 |
| 40 | HDIO0_10 | HDIO0_11 | HDIO0_12 | HDIO0_13 | HDIO0_14 |
| 41 | HDIO0_15 | HDIO0_16 | HDIO0_17 | HDIO0_18 | HDIO0/1_VCCO |
| 42 | HDIO0_19 | HDIO0_20 | HDIO0_21 | SPARE | HDIO0/1_VCCO |
| 43 | GND | GND | GND | GND | GND |
| 44 | GND | GND | GND | GND | GND |
| 45 | HDIO1_0 | HDIO1_1 | HDIO1_2 | HDIO1_3 | HDIO1_4 |
| 46 | HDIO1_5 | HDIO1_6 | HDIO1_7 | HDIO1_8 | HDIO1_9 |
| 47 | HDIO1_10 | HDIO1_11 | HDIO1_12 | HDIO1_13 | HDIO1_14 |
| 48 | HDIO1_15 | HDIO1_16 | HDIO1_17 | HDIO1_18 | HDIO0/1_VCCO |
| 49 | HDIO1_19 | HDIO1_20 | HDIO1_21 | SPARE | HDIO0/1_VCCO |
| 50 | GND | GND | GND | GND | GND |

- **Expansion Board Outline Dimension**



## M.2 E-Key Slot (M1) / M.2 M-Key Slot (M2)

The motherboard provides
One M.2 Slot M-key (PCIe 4.0 x4) with 2280 storage type for SSD
One M.2 Slot E-key (PCIe 4.0 x1 and USB2.0) with 2230 type for Wifi/BT




LED3:
When the M.2 slot is in Wifi mode, this Green LED is on.

LED4:
When the M.2 slot is in bluetooth mode, this Green LED is on.

M1:
M.2 2230 E-key for wifi/bluetooth

M2:
M.2 2280 M-key for M.2 SSD device

LED2:
When the M.2 SSD device is functional, this Green LED is blinking.

Note:
Recommended torque for the M.2 hold down screws: 1 ~ 1.5lbf·in.

- **M.2 E-Key Slot Installation**

To install the M.2 wifi/bluetooth card (type 2230):

1. Remove screws and align the notch on the M.2 wifi/bluetooth card edge connector with the tab in the slot.
2. Plug the M.2 wifi/bluetooth card firmly into the slot at a 20-degree angle, and until it clicks into place.
3. Fasten M.2 wifi/bluetooth card onto the nut with accompanied screws.

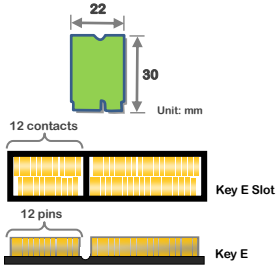









Note:
The motherboard in the picture is not actual motherboard, just for reference.




To reduce electromagnetic exposure, please maintain a minimum separation distance of 20 cm from the product during operation.

- **M.2 M-Key Slot Installation**

To install the M.2 SSD device (type 2280):

1. Remove screws and align the notch on the M.2 SSD device edge connector with the tab in the slot.
2. Plug the M.2 SSD device firmly into the slot at a 20-degree angle, and until it clicks into place.
3. Fasten M.2 SSD device onto the nut with accompanied screws.

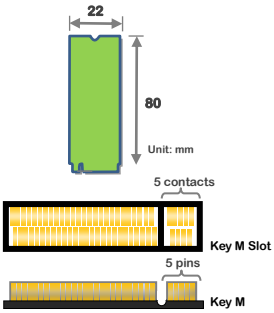









Note:
The motherboard in the picture is not actual motherboard, just for reference.




**Removing Device Caution**

- Remove the M.2 wifi/bluetooth card or M.2 SSD device at a 20-degree angle.
- Please DO NOT pull up the M.2 wifi/bluetooth card or M.2 SSD device to avoid damage to the M.2 slot.






## M.2 E-key 2230 – Supports PCIe x1 & USB2.0 based device interfaces

| Pin id. | Pin name | Description | Voltage |
|---|---|---|---|
| 1 | GND | Ground | |
| 2 | +3.3V | 3.3 V power supply | |
| 3 | USB_D+ | USB high-, full-, and low- speed data pair positive | |
| 4 | +3.3V | 3.3 V power supply | |
| 5 | USB_D- | USB high-, full-, and low- speed data pair negative | |
| 6 | LED1# | M2_WL_LED- | |
| 7 | GND | Ground | |
| 8 | PCM_CLK /I²S SCK | PCM Clock/ I²S Continuous Serial Clock (SCK) | 1.8 V |
| 9 | N/A | | |
| 10 | PCM_SYNC/I²S WS | PCM synchronous data SYNC/ I²Sword Select | 1.8 V |
| 11 | N/A | | |
| 12 | PCM_IN/I²S SD_IN | PCM synchronous data INput/ I²S Serial Data IN | 1.8 V |
| 13 | N/A | | |
| 14 | PCM_OUT/I²S_SD_OUT | PCM synchronous data OUTput/ I2S Serial Data OUT | 1.8 V |
| 15 | N/A | | |
| 16 | LED2# | M2_BT_LED- | |
| 17 | N/A | | |
| 18 | GND | Ground | |
| 19 | N/A | | |
| 20 | WAKE# | M2_BT_WAKE- | 0/3.3V |
| 21 | N/A | | |
| 22 | N/A | | |
| 23 | N/A | | |
| 24-31 | Key E | Substrate removed to act as physical key | |
| 32 | N/A | | |
| 33 | GND | Ground | |
| 34 | N/A | | |
| 35 | PETp0 | PCI Express lane 0 module transmitter pair positive | |
| 36 | N/A | | |
| 37 | PETn0 | PCI Express lane 0 module transmitter pair negative | |
| 38 | PEREFCLKP0 | BT_DEV_WAKE- | 0/3.3V |
| 39 | GND | Ground | |
| 40 | N/A | | |
| 41 | PERp0 | PCI Express lane 0 module receiver pair positive | |
| 42 | N/A | | |
| 43 | PERn0 | PCI Express lane 0 module receiver pair negative | |
| 44 | N/A | | |
| 45 | GND | Ground | |
| 46 | N/A | | |
| 47 | PEREFCLKP0 | PCI Express reference clock pair positive | |
| 48 | N/A | | |
| 49 | PEFCLKN0 | PCI Express reference clock pair negative | |
| 50 | SUSCLK | 32.768 kHz clock module input | 0/3.3V |
| 51 | GND | Ground | |
| 52 | PERST0# | PCI Express reset | 0/3.3V |
| 53 | CLKREQ0# | PCI Express clock request | 0/3.3V |
| 54 | W_DISABLE2# | Wireless disable 2 | 0/3.3V |
| 55 | PEWake0# | PCI Express wake | 0/3.3V |
| 56 | W_DISABLE1# | Wireless disable 1 | 0/3.3V |
| 57 | GND | Ground | |
| 58 | I2C_DATA | I2C data. Open Drain with pull up on Platform | 1.8 V |
| 59 | N/A | | |
| 60 | I2C_CLK | I2C clock input from host. Open Drain with pull up on Platform | 1.8 V |
| 61 | N/A | | |
| 62 | N/A | | |
| 63 | GND | Ground | |
| 64 | N/A | | |
| 65 | N/A | | |
| 66 | N/A | | |
| 67 | Reserved/PERn1 | | |
| 68 | N/A | | |
| 69 | GND | Ground | |
| 70 | N/A | | |
| 71 | N/A | | |
| 72 | +3.3V | power supply | 3.3 V |
| 73 | N/A | | |
| 74 | +3.3V | power supply | 3.3 V |
| 75 | GND | Ground | |

## M.2 M-key 2280– Supports PCIe x4 NVMe SSD Storage interfaces

| Pin id. | Pin name | Description | Voltage |
|---|---|---|---|
| 1 | NC | No Connect | |
| 2 | 3.3 V | Supply pin | 3.3 V |
| 3 | GND | Ground | |
| 4 | 3.3 V | Supply pin | 3.3 V |
| 5 | PERn3 | PCIe Lane 3 Rx | |
| 6 | N/A | | |
| 7 | PERp3 | PCIe Lane 3 Rx | |
| 8 | N/A | | |
| 9 | GND | Ground | |
| 10 | DAS/DSS | Device Activity Signal / Disable Staggered Spinup | |
| 11 | PETn3 | PCIe Lane 3 Tx | |
| 12 | 3.3 V | Supply pin | 3.3 V |
| 13 | PETp3 | PCIe Lane 3 Tx | |
| 14 | 3.3 V | Supply pin | 3.3 V |
| 15 | GND | Ground | |
| 16 | 3.3V | Supply pin | 3.3 V |
| 17 | PERn2 | PCIe Lane 2 Rx | |
| 18 | 3.3 V | Supply pin | 3.3 V |
| 19 | PERp2 | PCIe Lane 2 Rx | |
| 20 | N/A | | |
| 21 | GND | Ground | |
| 22 | N/A | | |
| 23 | PETn2 | PCIe Lane 2 Tx | |
| 24 | N/A | | |
| 25 | PETp2 | PCIe Lane 2 Tx | |
| 26 | N/A | | |
| 27 | GND | Ground | |
| 28 | N/A | | |
| 29 | PERn1 | PCIe Lane 1 Rx | |
| 30 | N/A | | |
| 31 | PERp1 | PCIe Lane 1 Rx | |
| 32 | N/A | | |
| 33 | GND | Ground | |
| 34 | N/A | | |
| 35 | PETn1 | PCIe Lane 1 Tx | |
| 36 | N/A | | |
| 37 | PETp1 | PCIe Lane 1 Tx | |
| 38 | N/A | | |
| 39 | GND | Ground | |
| 40 | N/A | | |
| 41 | SATA-B+/PERn0 | Host receiver differential signal pair. If in PCIe mode PCIe Lane 0 Rx | |
| 42 | N/A | | |
| 43 | SATA-B-/PERp0 | Host receiver differential signal pair. If in PCIe mode PCIe Lane 0 Rx | |
| 44 | N/A | | |
| 45 | GND | Ground | |
| 46 | N/A | | |
| 47 | SATA-A-/PETn0 | Host transmitter differential signal pair. If in PCIe mode PCIe Lane 0 Tx | |
| 48 | N/A | | |
| 49 | SATA-A+/PETp0 | Host transmitter differential signal pair. If in PCIe mode PCIe Lane 0 Tx | |
| 50 | PERST# | PCIe reset | |
| 51 | GND | Ground | |
| 52 | CLKREQ# | Reference clock request signal | |
| 53 | REFCLKN | PCIe Reference Clock signals (100 MHz) | |
| 54 | PEWAKE# | PCIe WAKE# Open Drain with pull up on platform. Active Low. | |
| 55 | REFCLKP | PCIe Reference Clock signals (100 MHz) | |
| 56 | N/A | | |
| 57 | GND | Ground | |
| 58 | N/A | | |
| 59-66 | removed (Key M) | Mechanical notch M | |
| 67 | N/A | | |
| 68 | SUSCLK | 32.768 kHz clock supply input provided by the Platform chipset | |
| 69 | CONFIG_1 | Defines module type (0 :SATA 1:NVME) | |
| 70 | 3.3 V | Supply pin | 3.3 V |
| 71 | GND | Ground | |
| 72 | 3.3 V | Supply pin | 3.3 V |
| 73 | GND | Ground | |
| 74 | 3.3 V | Supply pin | 3.3 V |
| 75 | GND | Ground | |

**Front Panel Header (CFP)**

The front panel header (2x5pin, 2.54mm pitch) on this motherboard is used to connect the front panel switches and LEDs.

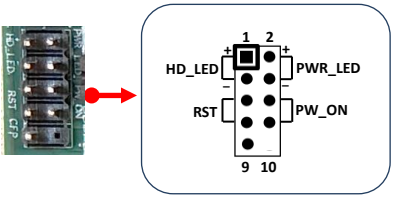
- PWR_LED
  Attach the front panel power LED cable to these two pins of the connector. The Power LED indicates the system's status.

| System Status | Power LED indicates |
|---|---|
| S0 | The LED is on |
| S5 | The LED is off |
| S3 | The LED will blink |
| S4 | The LED is off |

- PW_ON
  Attach the power button cable from the case to these two pins. Pressing the power button on the front panel turns the system on and off rather than using the onboard button.

- HD_LED
  Attach the hard disk drive indicator LED cable to these two pins. The HDD indicator LED indicates the activity status of the hard disks.

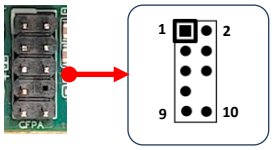
- RESET
  Attach the Reset switch cable from the front panel of the case to these two pins. The system restarts when the RESET switch is pressed.




| Header | Pin | Signal |
|---|---|---|
| HD_LED | 1 | HD_PWR |
| | 3 | HD Active |
| PWRLED | 2 | PWR LED+ |
| | 4 | PWR LED- |
| RESET | 5 | Ground |
| | 7 | RST BTN |
| PWRSW | 6 | PWR BTN |
| | 8 | Ground |
| No Connect | 9 | NC |
| Empty | 10 | Empty |

## CFPA Header (CFPA)

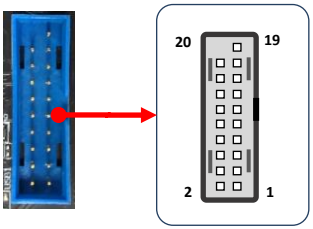
This header (2x5pin, 2.54mm pitch) allows you to connect the front panel audio. The audio connector supports HD audio standard.




| Pin | Definition | Pin | Definition |
|---|---|---|---|
| 1 | MIC_L | 2 | GND |
| 3 | MIC_R | 4 | NC |
| 5 | OUT_R | 6 | MIC_JD |
| 7 | IO_JD | 8 | Empty |
| 9 | OUT_L | 10 | OUT_JD |

## USB3.2 Gen 2 Header (USB32)

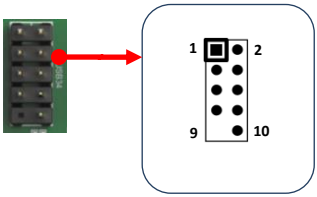
This motherboard contains one USB3.2 Gen 2 onboard header (2x10pin, 2.00mm pitch), supports data transfer rates up to 10Gbps that can be used to connect to two (2) external USB 2.0 devices.




| From USB Hub | | From APU | |
|---|---|---|---|
| Pin | Definition | Pin | Definition |
| 1 | NC | 2 | D1+ |
| 3 | D2+ | 4 | D1- |
| 5 | D2- | 6 | GND |
| 7 | GND | 8 | SSTX1+ |
| 9 | SSTX2+ | 10 | SSTX1- |
| 11 | SSTX2- | 12 | GND |
| 13 | GND | 14 | SSRX1+ |
| 15 | SSRX2+ | 16 | SSRX1- |
| 17 | SSRX2- | 18 | VBUS |
| 19 | VBUS | 20 | Empty |

## USB2.0 Header (USB34)

This motherboard contains one 2x5-pin onboard header (USB2, 2.54mm pitch) that can be used to connect to two (2) external USB 2.0 devices.



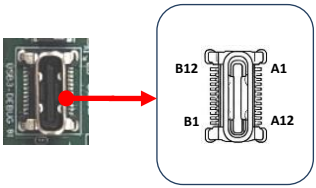

| Pin | Definition | Pin | Definition |
|---|---|---|---|
| 1 | VCC | 2 | VCC |
| 3 | USB0- | 4 | USB1- |
| 5 | USB0+ | 6 | USB1+ |
| 7 | GND | 8 | GND |
| 9 | Empty | 10 | No Connect |

### Internal USB INPUT Connector (USB3-DEBUG) (Select by JP6)

When the JP6 plug connects pins 1-2, the FPGA debug USB port source is from internal USB 2.0 port of APU.

When the JP6 plug connects pins 2-3, the FPGA debug USB port source is from an external computer through the USB Type C port (USB3-DEBUG connector).

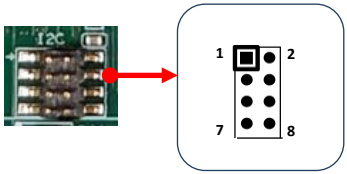
The user needs to supply a standard USB Type C to Type A cable for this connection.




| Pin | Definition | Pin | Definition |
|---|---|---|---|
| A1 | GND | B1 | GND |
| A2 | NC | B2 | NC |
| A3 | NC | B3 | NC |
| A4 | POWER | B4 | POWER |
| A5 | CC1 | B5 | NC |
| A6 | D+ | B6 | D- |
| A7 | D- | B7 | D+ |
| A8 | NC | B8 | CC2 |
| A9 | POWER | B9 | POWER |
| A10 | HSDP_RXN | B10 | HSDP_TXN |
| A11 | HSDP_RXP | B11 | HSDP_TXP |
| A12 | GND | B12 | GND |

### I2C Header (I2C)

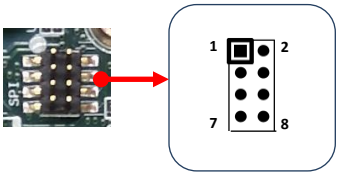
The I2C header (2x4pin, 1.27mm pitch) is for access to the I2C communication bus.




| Pin | Definition | Pin | Definition |
|---|---|---|---|
| 1 | I2C_A0 | 2 | VCC |
| 3 | I2C_A1 | 4 | I2C_WP |
| 5 | I2C_A2 | 6 | PMC_MIO42_I2C0_SCL |
| 7 | GND | 8 | PMC_MIO43_I2C0_SDA |

### SPI Header (SPI)

The SPI header (2x4pin, 1.27mm pitch) is for SPI signal interface.

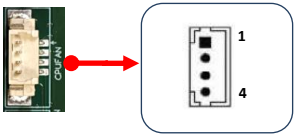



| Pin | Definition | Pin | Definition |
|---|---|---|---|
| 1 | SPI_POWER | 2 | GND |
| 3 | SPI_CS- | 4 | SPI_CLK |
| 5 | SPI_DATAIN | 6 | SPI_DATAOUT |
| 7 | NC | 8 | DediProg_L |

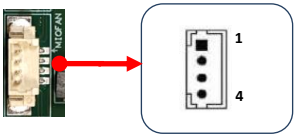
### Fan Headers (CPUFAN/MIOFAN/SYSFAN)

There are three headers (CPUFAN/MIOFAN 1x4pin 1.25mm pitch and SYSFAN 1x4pin 2.54mm pitch) on the motherboard.
CPUFAN header provides power and control to the CPU cooler fan.
MIOFAN header provides power and control to the FPGA cooler fan.
SYSFAN header provides power and control to the chassis fan.

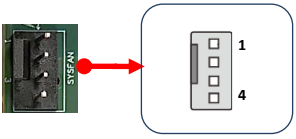
These fans can be speed detected/controlled and displayed in the Hardware Monitor > Smart Fan Function menu of the BIOS Setup. The fans are automatically turned off after the system enters S3, S4 or S5 mode.




| Pin | Definition |
|---|---|
| 1 | GND |
| 2 | +12V |
| 3 | Sense |
| 4 | Control |



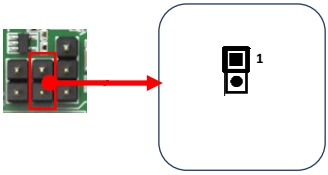

| Pin | Definition |
|---|---|
| 1 | GND |
| 2 | +12V |
| 3 | Sense |
| 4 | Control |




| Pin | Definition |
|---|---|
| 1 | GND |
| 2 | +12V |
| 3 | Sense |
| 4 | Control |

### 2VE3558 GPIO1 Header (J3)

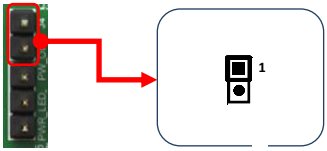
This header (1x2pin, 2.54mm pitch)




| Pin | Definition |
|---|---|
| 1 | FuSa_GPIO1 |
| 2 | GND |

### 2VE3558 GPIO2 Header (J4)

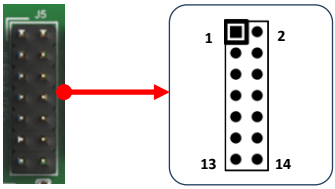
This header (1x2pin, 2.54mm pitch)




| Pin | Definition |
|---|---|
| 1 | FuSa_GPIO2 |
| 2 | GND |

### AMD FPGA JTAG Port (J5, Internal Use Only)

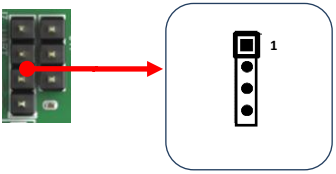
This header (2x7pin, 2.0mm pitch)




| Pin | Definition | Pin | Definition |
|---|---|---|---|
| 1 | GND | 2 | +1.8V |
| 3 | GND | 4 | VE3558_TMS |
| 5 | GND | 6 | VE3558_TCK |
| 7 | GND | 8 | VE3558_TDO |
| 9 | GND | 10 | VE3558_TDI |
| 11 | GND | 12 | NC |
| 13 | GND | 14 | RESET- |

### UART Header (J7)

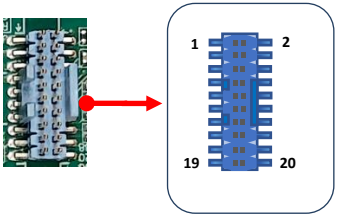
This header (1x4pin, 2.54mm pitch) is a serial interface for debugging.




| Pin | Definition |
|---|---|
| 1 | +3.3V |
| 2 | HDR_UART0_TXD |
| 3 | HDR_UART0_RXD |
| 4 | GND |

### AMD APU HDT+ Header (J8, Internal Use Only)

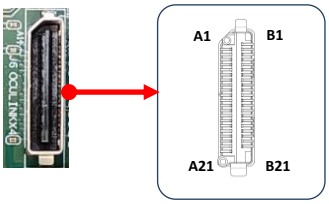
This header (2x10pin, 1.27mm pitch)




| Pin | Definition | Pin | Definition |
|---|---|---|---|
| 1 | +1.8V_ALW | 2 | APU_TCK |
| 3 | GND | 4 | APU_TMS |
| 5 | GND | 6 | APU_TDI |
| 7 | GND | 8 | APU_TDO |
| 9 | APU_TRST- | 10 | APU_PWRGD |
| 11 | GND | 12 | RESET- |
| 13 | GND | 14 | NC |
| 15 | GND | 16 | APU_DBREQ- |
| 17 | GND | 18 | NC |
| 19 | +1.8V_ALW | 20 | NC |

## OCULINKX4 Connector (J15)

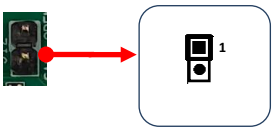
This header (42pin) is a peripheral connection standard that allows you to connect PCIe devices using an external cable.




| Pin | Definition | Pin | Definition |
|---|---|---|---|
| A1 | +3.3V | B1 | +5V |
| A2 | GND | B2 | GND |
| A3 | GFX_RX0P | B3 | GFX_TX0P |
| A4 | GFX_RX0N | B4 | GFX_TX0N |
| A5 | GND | B5 | GND |
| A6 | GFX_RX1P | B6 | GFX_TX1P |
| A7 | GFX_RX1N | B7 | GFX_TX1N |
| A8 | GND | B8 | GND |
| A9 | NC | B9 | NC |
| A10 | PCIE_WAKE_UP | B10 | NC |
| A11 | GND | B11 | GND |
| A12 | GFX_CLKP | B12 | PCIE_RST |
| A13 | GFX_CLKN | B13 | CPRSNT- |
| A14 | GND | B14 | GND |
| A15 | GFX_RX2P | B15 | GFX_TX2P |
| A16 | GFX_RX2N | B16 | GFX_TX2N |
| A17 | GND | B17 | GND |
| A18 | GFX_RX3P | B18 | GFX_TX3P |
| A19 | GFX_RX3N | B19 | GFX_TX3N |
| A20 | GND | B20 | GND |
| A21 | +5V | B21 | +3.3V |

## Case Open Header (J17)

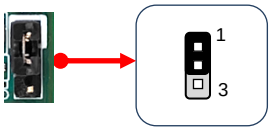
This header (1x2pin, 2.54mm pitch) is for a chassis open detect. When set, the warning message will appear during POST when the case is opened.




| Pin | Definition |
|---|---|
| 1 | Case Open |
| 2 | GND |

## Versal2 Power Control Jumper (JP1)

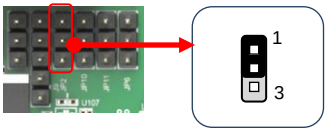
You can use JP1 (1x3pin, 2.54mm pitch) for Versal Power Control.




| Pin | Settings |
|---|---|
| 1-2 | Enable All of Versal2 Power (Default) |
| 2-3 | Disable All of Versal2 Power |

### ROM Write Protect mode Jumper (JP2)

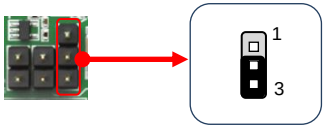
You can use JP2 (1x3pin, 2.54mm pitch) for ROM Write Protect mode selection.




| Pin | Settings |
|---|---|
| 1-2 | Write Protect (Default) |
| 2-3 | Write Operations |

### FUSE Power Control Jumper (JP3)

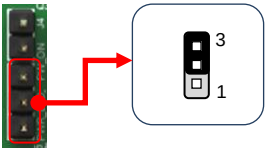
You can use JP3 (1x3pin, 2.54mm pitch) to enable or disable the FUSE Power Control function.




| Pin | Settings |
|---|---|
| 1-2 | Enable Burn the FUSE |
| 2-3 | Disable Burn the FUSE (Default) |

### Auto Power ON Jumper (JP4)

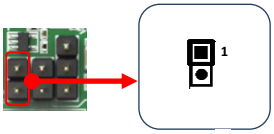
You can use JP4 (2.54mm pitch) to select to enable or disable the auto power on function.




| Pin | Settings |
|---|---|
| 1-2 | Disable.<br>Press power button manually to power on after power input is connected to power source |
| 2-3 | Enable.<br>Automatically power on when power input is connected to power source (Default) |

### 2VE3558 MODE Selection Jumper (JP5)

You can use JP5 (1x2pin, 2.54mm pitch) for 2VE3558 MODE selection.




| Pin | Settings |
|---|---|
| NC | OSPI Mode (Default) |
| POP | JTAG Mode |

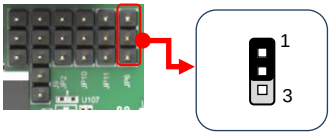
### USB Debug Port Selection Jumper of 2VE3558 (JP6)

The AMD Versal AI Edge Gen2 2VE3558 FPGA is connected to a USB 2.0 interface via an FTDI FT4232 USB-to-JTAG/USB-UART device, providing access for debugging purposes.

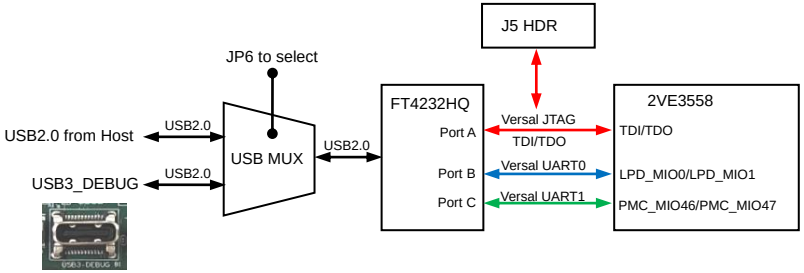
There are two debug USB port that are selected by JP6.

When the JP6 plug connects pins 1-2, the FPGA debug USB port source is from internal USB 2.0 port of APU.

When the JP6 plug connects pins 2-3, the FPGA debug USB port source is from an external computer through the USB Type C port (USB3-DEBUG connector).



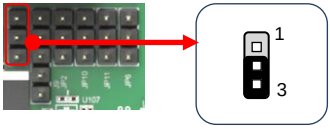

| Pin | Settings |
|---|---|
| 1-2 | Internal USB (Default) |
| 2-3 | External USB (connect from USB3-DEBUG) |




| FT4232HQ (U110) | Versal Device (U28) |
|---|---|
| Port AD JTAG | 2VE3558 JTAG Chain |
| Port BD UART0 | UART0: LPD_MIO0/LPD_MIO1 |
| Port CD UART1 | UART1: PMC_MIO46/PMC_MIO47 |

### MDIO Select Jumper (JP7)

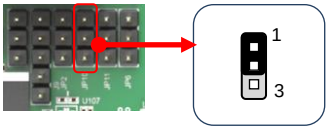
You can use JP7 (1x3pin, 2.54mm pitch) for MDIO selection.




| Pin | Settings |
|---|---|
| 1-2 | CPU Managed of CPU is Attached |
| 2-3 | No CPU Attached (Default) |

### UART Select Jumper (JP10)

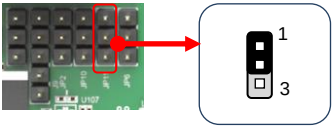
You can use JP10 (1x3pin, 2.54mm pitch) for UART selection.




| Pin | Settings |
|---|---|
| 1-2 | FTDI UART (Default) |
| 2-3 | Ryzen to Versal2 UART |

### Versal2 JTAG Jumper (JP11)

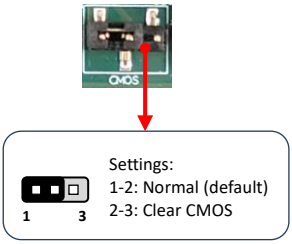
You can use JP11 (1x3pin, 2.54mm pitch) to enable or disable the Versal2 JTAG function.




| Pin | Settings |
|---|---|
| 1-2 | Disabled (Default) |
| 2-3 | Enabled |

### Clear CMOS Jumper (CMOS)

This motherboard contains a jumper (CMOS, 1x3pin 2.54mm pitch) that can clear CMOS data. If the CMOS data becomes corrupted or you forgot the supervisor or user password, clear the CMOS data to reconfigure the system back to the default values stored in the ROM BIOS.

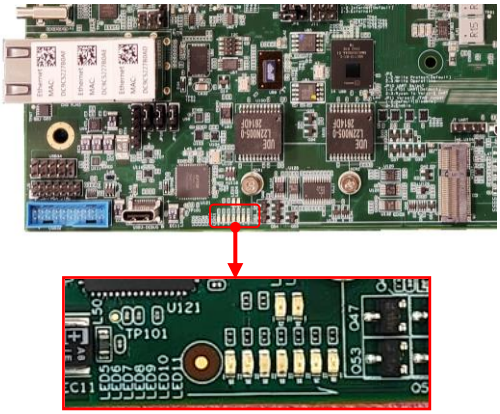



To clear CMOS data, please follow the steps below.

1. Turn off the system.
2. Change the jumper from “1-2” to “2-3” position for a few seconds.
3. Replace the jumper back to the “1-2” position.
4. Turn on the system and hold down the <Del> or <F2> key to enter BIOS Setup.

## 3.3 Onboard LED Status Indicators

This motherboard provides several LEDs to indicate the system's status.

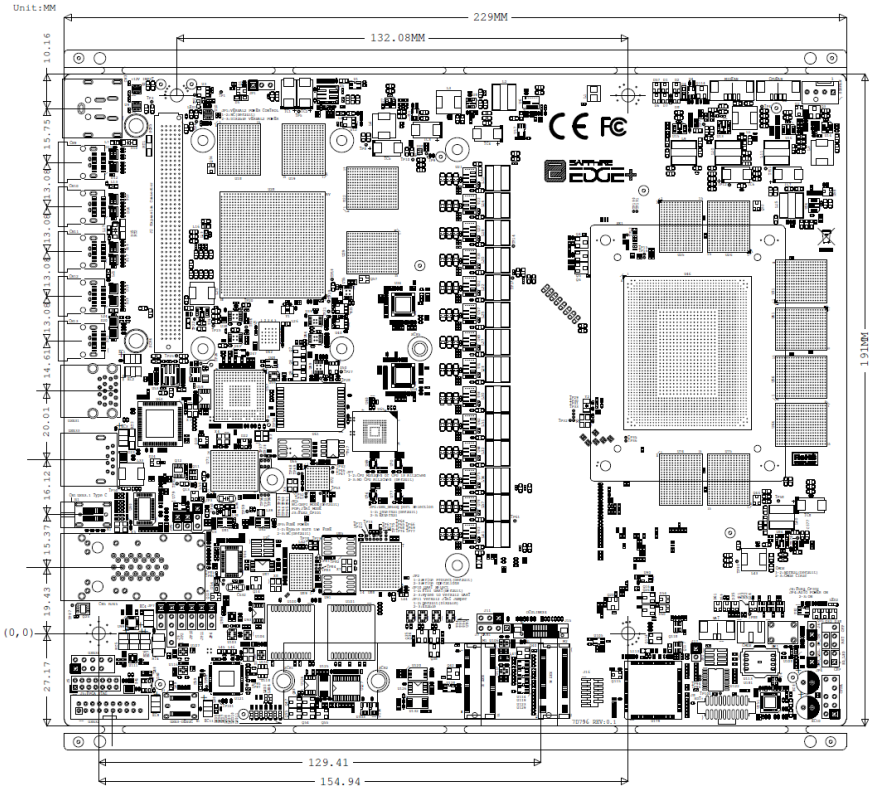



**LED5 ~ LED11**

| LED# | Color | Function description |
|---|---|---|
| LED5 | Green | FP11 Power LED |
| LED6 | Blue | FP11 Standby Power LED |
| LED7 | Yellow | FP11 Memory Power LED |
| LED8 | Red | VERSAL2_ERROR_OUT LED |
| LED9 | Green | VERSAL2 DONE LED |
| LED10 | Green | APU Status LED |
| LED11 | Green | VERSAL2 RPU Status LED |

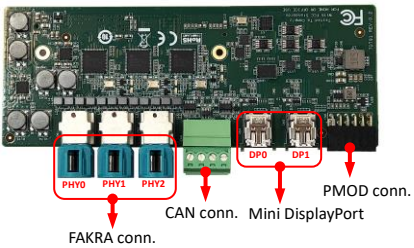
## *3.4 Motherboard Dimension*

PCB Size: 191 x 229mm

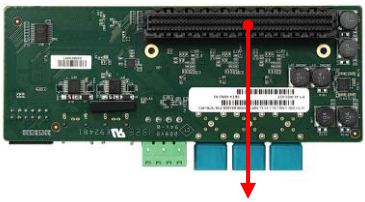


## 3.5 AUTO I/O BOARD *(GMSL2 x3, CAN x2, mDP x2, PMOD Header)*

**Front View**



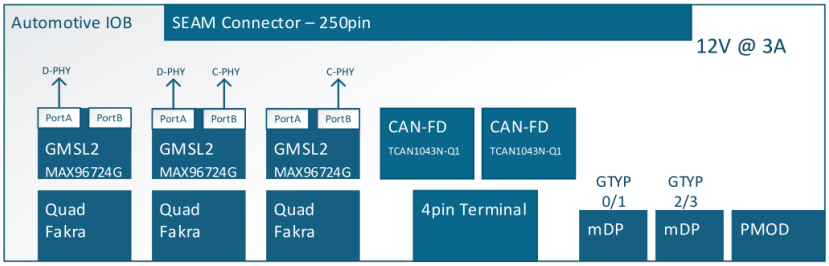

**Back View**




The Automotive I/O Daughter Board is designed to extend the functionality of the RAVE2 platform by providing automotive camera, networking, display, and general-purpose I/O interfaces.

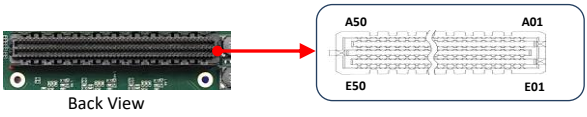
Connected through the RAVE2 expansion connector, the board supports up to twelve GMSL2 cameras through FAKRA connectors and MIPI C-PHY interfaces to the AMD Versal Edge Gen2 device. In addition, the board provides dual CAN-FD interfaces, HDIO-based GPIO and I2C expansion, a PMOD connector for peripheral evaluation, and dual DisplayPort outputs through the Versal GT transceivers.

The Automotive I/O Daughter Board enables rapid development and evaluation of automotive vision, sensor fusion, vehicle communication, and edge AI applications on the RAVE2 platform.




<Function block diagram>

## ❒ J1 SEAM connector pinout



Back View

### ● IO Expansion connector pin map (GMSL2)

PHY0

| Pin # | I/O Bank | PHY # | PHY Signals |
|---|---|---|---|
| A26 | O0P6_GCP | 0 | PHY0_DA2P |
| A27 | O0P7_GCN | 0 | PHY0_DA2N |
| A29 | O0P0_DATAP | 0 | PHY0_DA0P |
| A30 | O0P1_DATAN | 0 | PHY0_DA0N |
| A32 | O1P0_DATAP | 0 | PHY0_DA3P |
| A33 | O1P1_DATAN | 0 | PHY0_DA3N |
| A38 | 400_HDIO5 | 0 | PT_I2C_SCL_0 |
| A39 | 400_HDIO10 | 0 | PWDNB_0 |
| B29 | O0P2_CLKP | 0 | PHY0_CKAP |
| B30 | O0P3_CLKN | 0 | PHY0_CKAN |
| B38 | 400_HDIO1 | 0 | PT_I2C_SDA_0 |
| B42 | 400_HDIO20 | 0 | PHY0_GPIO1 |
| C29 | O0P4_DATAP | 0 | PHY0_DA1P |
| C30 | O0P5_DATAN | 0 | PHY0_DA1N |
| C38 | 400_HDIO2 | 0 | PHY0_MFP5_ERRB |
| C42 | 400_HDIO21 | 0 | PHY0_GPIO0 |
| D38 | 400_HDIO3 | 0 | PHY0_MFP4_LOCK |

PHY1

| Pin # | I/O Bank | PHY # | PHY Signals | Pin # | I/O Bank | PHY # | PHY Signals |
|---|---|---|---|---|---|---|---|
| A17 | O0P0_A0A | 1 | PHY1_CB0A | C39 | 400_HDIO7 | 1 | PT_I2C_SDA_1 |
| A18 | O0P1_A0B | 1 | PHY1_CB0B | D17 | O1P6_A3A | 1 | PHY1_CB3A |
| A20 | O1P0_A2A | 1 | PHY1_CB2A | D18 | O1P7_A3B | 1 | PHY1_CB3B |
| A21 | O1P1_A2B | 1 | PHY1_CB2B | D20 | O0P6_A1A | 1 | PHY1_CB1A |
| A35 | O2P0_DATAP | 1 | PHY1_DA0P | D21 | O0P7_A1B | 1 | PHY1_CB1B |
| A36 | O2P1_DATAN | 1 | PHY1_DA0N | D35 | O2P6_DATAP | 1 | PHY1_DA2P |
| A40 | 400_HDIO10 | 1 | PWDNB_1 | D36 | O2P7_DATAN | 1 | PHY1_DA2N |
| B17 | O0P2_A0C | 1 | PHY1_CB0C | D39 | 400_HDIO13 | 1 | PHY1_MFP4_LOCK |
| B20 | O1P2_A2C | 1 | PHY1_CB2C | E35 | O3P0_DATAP | 1 | PHY1_DA3P |
| B35 | O2P2_CLKP | 1 | PHY1_CKAP | E36 | O3P1_DATAN | 1 | PHY1_DA3N |
| B36 | O2P3_CLKN | 1 | PHY1_CKAN | E38 | 400_HDIO4 | 1 | PT_I2C_SCL_1 |
| B39 | 400_HDIO6 | 1 | PHY1_GPIO0 | E39 | 400_HDIO9 | 1 | PHY1_GPIO1 |
| B40 | 400_HDIO11 | 1 | PHY1_MFP5_ERRB | | | | |
| C17 | O1P4_A3C | 1 | PHY1_CB3C | | | | |
| C20 | O0P4_A1C | 1 | PHY1_CB1C | | | | |
| C35 | O2P4_DATAP | 1 | PHY1_DA1P | | | | |
| C36 | O2P5_DATAN | 1 | PHY1_DA1N | | | | |

## PHY2

| Pin # | I/O Bank | PHY # | PHY Signals |
|---|---|---|---|
| A23 | O2P0_B0A | 2 | PHY2_CB0A |
| A24 | O2P1_B0B | 2 | PHY2_CB0B |
| A41 | 400_HDIO15 | 2 | PHY2_GPIO0 |
| A42 | 400_HDIO19 | 2 | PWDNB_2 |
| B23 | O2P2_B0C | 2 | PHY2_CB0C |
| B41 | 400_HDIO16 | 2 | PHY2_MFP5_ERRB |
| C23 | O2P4_B1C | 2 | PHY2_CB1C |
| C40 | 400_HDIO12 | 2 | PT_I2C_SCL_2 |
| C41 | 400_HDIO17 | 2 | PHY2_MFP4_LOCK |
| D23 | O2P6_B1A | 2 | PHY2_CB1A |
| D24 | O2P7_B1B | 2 | PHY2_CB1B |
| D40 | 400_HDIO13 | 2 | PT_I2C_SDA_2 |
| E17 | O3P0_B2A | 2 | PHY2_CB2A |
| E18 | O3P1_B2B | 2 | PHY2_CB2B |
| E20 | O3P2_B2C | 2 | PHY2_CB2C |
| E24 | O3P4_B3C | 2 | PHY2_CB3C |
| E26 | O3P6_B3A | 2 | PHY2_CB3A |
| E27 | O3P7_B3B | 2 | PHY2_CB3B |
| E40 | 400_HDIO14 | 2 | PHY2_GPIO1 |

## Power PIN

| Pin # | I/O Bank | POWER | POWER DOMAIN |
|---|---|---|---|
| A1 | | +12V | CNCTR_12V |
| B1 | | +12V | CNCTR_12V |
| C1 | | +12V | CNCTR_12V |
| D1 | | +12V | CNCTR_12V |
| E1 | | +12V | CNCTR_12V |
| B26 | BANK 709 | +1.2V | VCCO_X5IO_709 |
| B27 | BANK 709 | +1.2V | VCCO_X5IO_709 |
| D26 | BANK 708 | +1.2V | VCCO_X5IO_708 |
| D27 | BANK 708 | +1.2V | VCCO_X5IO_708 |
| E41 | BANK 400 | +1.8V | VCCO_400_HDIO |
| E42 | BANK 400 | +1.8V | VCCO_400_HDIO |
| E48 | BANK 400 | +1.8V | VCCO_400_HDIO |
| E49 | BANK 400 | +1.8V | VCCO_400_HDIO |

- **IO Expansion connector pin map (CAN FD)**

| Pin # | Signals | PHY# | Host Signals |
|---|---|---|---|
| A3 | BOARD _PWR_EN | | PMC_MIO20 |
| A4 | CAN0_TX | 0 | PMC_MIO44 |
| A45 | CAN0EN | 0 | 401_HDIO0 |
| A46 | CAN0STB | 0 | 401_HDIO5 |
| B3 | CAN0_WK | 0 | PMC_MIO14 |
| B4 | CAN0_RX | 0 | PMC_MIO45 |
| C4 | CAN1_TX | 1 | PMC_MIO41 |
| D3 | CAN1_WK | 1 | PMC_MIO15 |
| D4 | CAN1_RX | 1 | PMC_MIO40 |
| D47 | CAN1EN | 1 | 401_HDIO13 |
| E47 | CAN1STB | 1 | 401_HDIO14 |

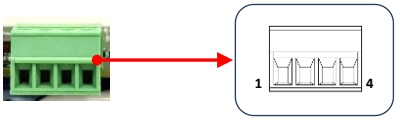
- **IO Expansion connector pin map (PMOD GPIO)**

| Pin # | Signals | Host Signals |
|---|---|---|
| A47 | CN6_PIN1 | 401_HDIO10 |
| A48 | CN6_PIN3 | 401_HDIO15 |
| A49 | CN6_PIN5 | 401_HDIO19 |
| B47 | CN6_PIN7 | 401_HDIO11 |
| B48 | CN6_PIN2 | 401_HDIO16 |
| B49 | CN6_PIN4 | 401_HDIO20 |
| C47 | CN6_PIN6 | 401_HDIO12 |
| C48 | CN6_PIN8 | 401_HDIO17 |

- **IO Expansion connector pin map (DP)**

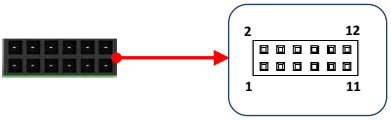
| Pin # | Signals | PHY# | Host Signals |
|---|---|---|---|
| A11 | DP0_GTYP_TXP1 | 0 | GTYP_TXP1 |
| A12 | DP0_GTYP_TXN1 | 0 | GTYP_TXN1 |
| A7 | DP0_GTYP_TXP0 | 0 | GTYP_TXP0 |
| A8 | DP0_GTYP_TXN0 | 0 | GTYP_TXN0 |
| B10 | DP1_GTYP_TXN0 | 1 | GTYP_TXN2 |
| B13 | DP1_GTYP_TXP1 | 1 | GTYP_TXP3 |
| B14 | DP1_GTYP_TXN1 | 1 | GTYP_TXN3 |
| B45 | DP0_AUX_OUT | 0 | 401_HDIO1 |
| B46 | DP0_AUX_IN | 0 | 401_HDIO6 |
| B9 | DP1_GTYP_TXP0 | 1 | GTYP_TXP2 |
| C11 | GTYP_CLKP1 | 1 | GTYP_CLKP1 |
| C12 | GTYP_CLKN1 | 1 | GTYP_CLKN1 |
| C45 | DP0_OE | 0 | 401_HDIO2 |
| C46 | DP0_HPD | 0 | 401_HDIO7 |
| C7 | GTYP_CLKP0 | 0 | GTYP_CLKP0 |
| C8 | GTYP_CLKN0 | 0 | GTYP_CLKN0 |
| D45 | DP1_AUX_OUT | 1 | 401_HDIO3 |
| D46 | DP1_AUX_IN | 1 | 401_HDIO8 |
| E3 | I2C1_SCL | | PMC_MIO16 |
| E4 | I2C1_SDA | | PMC_MIO17 |
| E45 | DP1_OE | 1 | 401_HDIO4 |
| E46 | DP1_HPD | 1 | 401_HDIO9 |

## ❒ CAN connector pinout




| Pin # | Signals |
|---|---|
| 1 | CAN1L |
| 2 | CAN1H |
| 3 | CAN0L |
| 4 | CAN0H |

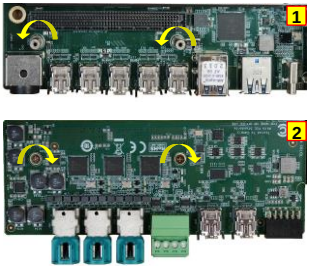
## ❒ PMOD connector pinout




| Pin # | Signals | Pin # | Signals |
|---|---|---|---|
| 1 | GPIO1 | 7 | GPIO7 |
| 2 | GPIO2 | 8 | GPIO8 |
| 3 | GPIO3 | 9 | GND |
| 4 | GPIO4 | 10 | GND |
| 5 | GPIO5 | 11 | +3.3V |
| 6 | GPIO6 | 12 | +3.3V |

To install the Auto I/O Daughter Board:

1. Remove two nuts from motherboard (as shown in the picture).
2. Align the board with the I/O Expansion Board Socket of motherboard and press down on the board until it is completely seated in the slot. Fasten IOB Board with nuts.



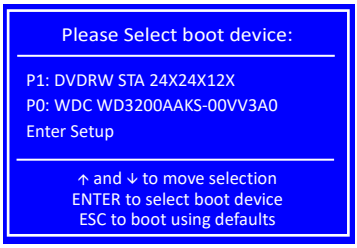
# Chapter 4 Configuring the BIOS

This chapter provides information on the BIOS Setup program and allows you to configure the system for optimum use.

## *4.1 Select Boot Device*

Select Boot Device Menu allows you to set the first boot device without entering BIOS Setup.

During Power On Self Test (POST), you can press the <**F7**> key to enter select boot device menu. The system will directly boot from the device configured in Boot Menu.




## *4.2 Enter BIOS Setup*

The BIOS is the communication bridge between hardware and software. Correctly setting the BIOS parameters is critical to maintain optimal system performance.

Use the following procedure to change BIOS settings.

1. Power on the computer.
2. Press the <**Del**> or <**F2**> key to enter BIOS Setup during BIOS Power On Self Test (POST).

Note1: You do not "need" to update the BIOS when receiving your system - it is shipped with working BIOS setting.

Note2: It is strongly recommended that you do not change the default BIOS settings. Changing some settings could damage your computer.

Note3: The BIOS options in this manual are for reference only. BIOS screens

in manuals are usually the first BIOS version when the board is released and may be different from your purchased motherboard. Users are welcome to download the latest BIOS version from our official website.

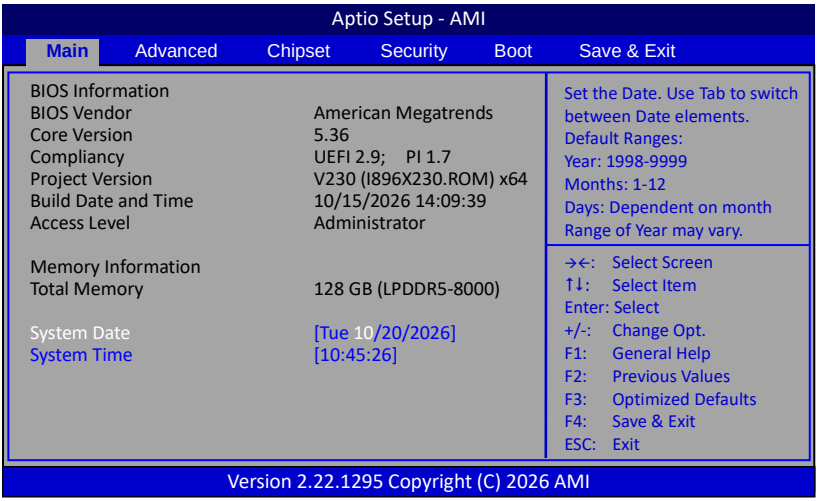
### Control Keys

Please check the following table for the function description of each Control key.

| Control Key(s) | Function Description |
|---|---|
| → / ← | Moves cursor left or right to select screens |
| ↑ / ↓ | Moves cursor up or down to select items |
| <Enter> | To bring up the selected item |
| + / - | To change option for the selected items |
| <F1> | To display the General Help Screen |
| <F2> | To load previous values for all the settings |
| <F3> | To load optimized default values for all the settings |
| <F4> | To save changes and exit the setup utility |
| <ESC> | To jump to the Exit Screen or exit the current screen |

## *4.3 Main Menu*

When entering the Aptio Setup Utility, the main menu screen appears. This main menu includes the system overview and displays the basic system configuration, such as BIOS information, memory size and system date/time.




**BIOS Information**

This field displays the current BIOS version, build date and ID information etc..

**Memory Information**

Displays current system memory size.

**System Date**

Allows you to set the system date.The format is <Day><Month><Date><Year>.

[Day] Weekday from Sun. to Sat., this is automatically displayed by BIOS.

[Month] The month from 1 to 12.

[Date] The date from 1 to 31 can be keyed by numeric function keys.

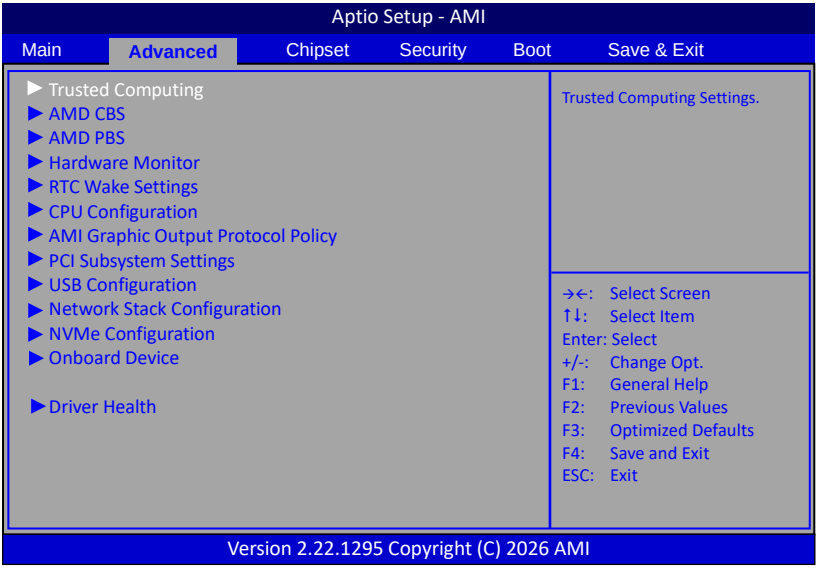
[Year] The year can be adjusted by users.

**System Time**

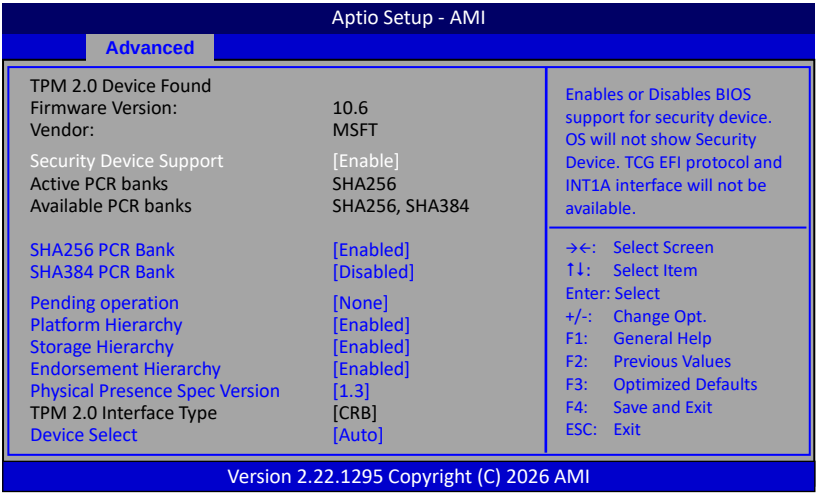
Allows you to set the system time. The time format is <hour>:<minute>:<second>.

## *4.4 Advanced Menu*

The Advanced menu items allow you to change the settings for the CPU, USB and other system devices. Press <Enter> to display the configuration options.




### ▶ Trusted Computing



**Security Device Support**
Enables or disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available. When enabled, the related items will appear.
Options: Enabled, Disabled.

**SHA256 PCR Bank**
Enable or disable SHA256 PCR Bank.
Options: Enabled, Disabled.

**SHA384 PCR Bank**
Enable or disable SHA384 PCR Bank.
Options: Enabled, Disabled.

**Pending operation**
Schedule an Operation for the Security Device.
NOTE: Your Computer will reboot during restart in order to change State of Security Device.
Options: None, TPM Clear.

**Platform Hierarchy**
Enables or disable Platform Hierarchy.
Options: Enabled, Disabled.

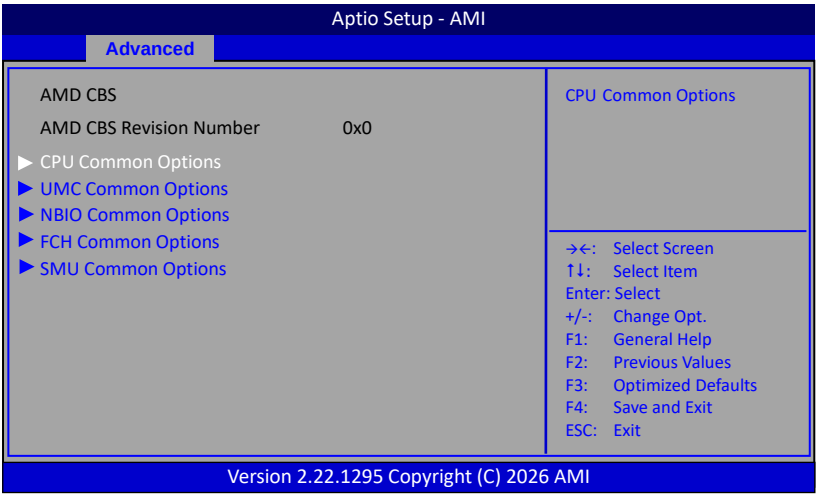
**Storage Hierarchy**
Enables or disable Storage Hierarchy.
Options: Enabled, Disabled.

**Endorsement Hierarchy**
Enables or disable Endorsement Hierarchy.
Options: Enabled, Disabled.

**Physical Presence Spec Version**
Select to Tell 0.S. to support PPI Spec version 1.2 or 1.3. Note some HCK tests might not support 1.3.
Options: 1.2, 1.3.

**Device Select**
TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated.
Options: TPM 1.2, TPM 2.0, Auto.

## ▶ AMD CBS




### ▶ CPU Common Options

**Core Performance Boost**

Allows the CPU to automatically increase its speed above the base clock when handling demanding tasks.

Options: Disabled, Auto.

**Global C-state Control**

Allows you controls IO based C-state generation and DF C-states. There is another DF C-state option which will be synchronized with this option if DF C-state option is auto.

Options: Enabled, Disabled, Auto.

**AVX512**

Allows you enable or disable CPU AVX512 control.

Options: Enabled, Disabled, Auto.

## UMC Common Options

### LPDDR Options

#### LPDDR Timing Configuration

Operating your AMD processor outside of specification or in excess of factory settings, including but not limited to overclocking, may damage or shorten the life of your processor or other system components, create system instabilities (e.g., data loss and corrupted images) and in extreme cases may result in total system failure. AMD does not provide support or service for issues or damages related to use of an AMD processor outside of processor specifications or in excess of factory settings.

**WARNING** - DAMAGE CAUSED BY USE OF YOUR AMD PROCESSOR OUTSIDE OF SPECIFICATION OR IN EXCESS OF FACTORY SETTINGS ARE NOT COVERED UNDER YOUR AMD PRODUCT WARRANTY AND MAY NOT BE COVERED BY YOUR SYSTEM MANUFACTURER'S WARRANTY.

#### LPDDR Security

**TSME**

Allow you to enable or disable the TSME (Transparent Secure Memory Encryption) function.
Options: Auto, Enabled, Disabled.

**Data Scramble**

Allow you to enable or disable Data Scramble function.
Options: Auto, Enabled, Disabled.

## NBIO Common Options

**IOMMU**

This item allows you to enable or disable the IOMMU (Input/Output Memory Management Unit).
Options: Disabled, Enabled, Auto.

**PCIe ARI Support**

This item allows you to enable or disable the PCIe ARI (Alternative Routing-ID Interpretation) support.
Options: Disabled, Enabled, Auto.

**GFX Configuration**

**iGPU Advanced Control**
Allows you to select the UMA mode.
Options: Enabled, Disabled, iGPU Disabled.

**iGPU Mem Bar Configuration**
Allows you to set the iGPU Mem Bar configuration.
LegacyGfxBAR: 256 MB or same as UMA carveout size for smaller carveout sizes in MMIO hole.
LargeBAR: same size as carveout ResizableBAR:256 MB BAR in MMIO hole and Resizable BAR for full carveout size enabled.
Options: Auto, LegacyGfxBAR, LargeBAR, ResizableBAR.

**UMA Version**
Allows you to select the UMA version.
Options: Legacy, Non-Legacy, Auto.

**GPU Host Translation Cache**
Allows you to enable or disable GPU Host Translation Cache.
Options: Auto, Enabled, Disabled.

**TCON INSTANT ON LOGO**
Allows you to enables or disables the instant display of the logo upon boot.
Options: Auto, Enabled, Disabled.

**Dedicated Graphics Memory**
Allows you to select the UMA frame buffer size level.
Options: 0.5G, 1G, 2G, 4G, 8G, 16G, 32G, 64G, 96G.

**Remaining System Memory**
Displays the remaining system memory size.

**PSPP Policy**
This item allows you to select PCIe speed power policy.
Options: Auto, Disabled, Balanced.

## FCH Common Options

### I3C/I2C Configuration Options

**I3C/I2C 0 Enable / I3C/I2C 1 Enable / I3C/I2C 2 Enable / I3C/I2C 3 Enable**

Enable or disable Inter-Integrated circuit control.
Options: Both Disabled, I3C Enabled, I2C Enabled, Auto.

### Uart Configuration Options

**Uart 0 Enable**

Enable or disable the UART 0. The UART 0 has no HW FC if UART 1 is enabled.
Options: Auto, Disabled, Enabled.

**Uart 0 Legacy Options**

Allow you to configure the UART 0 controller to act as a legacy COM port.
Options: Auto, Disabled, 0x2E8, 0x2F8, 0x3E8, 0x3F8.

**Uart 1 Enable (no HW FC)**

Enable or disable the UART 1.
Options: Auto, Disabled, Enabled.

**Uart 1 Legacy Options**

Allow you to configure the UART 1 controller to act as a legacy COM port.
Options: Auto, Disabled, 0x2E8, 0x2F8, 0x3E8, 0x3F8.

**Uart 2 Enable**

Enable or disable the UART 2. The UART 2 has no HW FC if UART 2 is enabled.
Options: Auto, Disabled, Enabled.

**Uart 2 Legacy Options**

Allow you to configure the UART 2 controller to act as a legacy COM port.
Options: Auto, Disabled, 0x2E8, 0x2F8, 0x3E8, 0x3F8.

**Uart 4 Enable**

Enable or disable the UART 4.
Options: Auto, Disabled, Enabled.

**SPI Configuration Options**

**HFP Enable**
Enable or disable the HFP (Hands-Free Profile) support.
Options: Auto, Disabled, Enabled.

**HID Enable / HID2 Enable**
Enable or disable the Human Interface Device (HID) support.
Options: Auto, Disabled, Enabled.

**HID2 Spi Read Mode**
Allows you to select the HID2 SPI read mode.
Options: Quad IO 1-4-4, Dual IO 1-2-2, Fast Read 1-1-1.

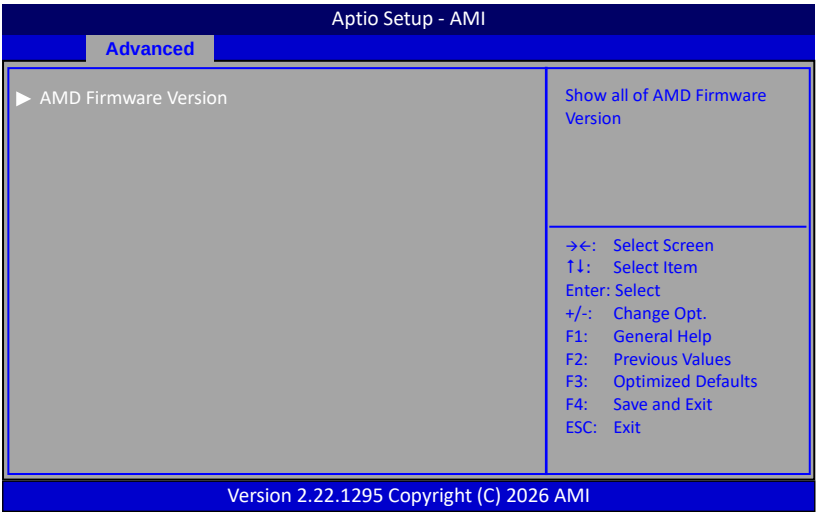
**HID2 Spi Speed**
Allows you to select the HID2 SPI speed.
Options: (1) 33MHz, (2) 22MHZ, (3) 17.6Mhz, (5) 800khz, spi_spd6, spi_spd7.

▶ **SMU Common Options**

**System Configuration**
This item allows you to select the system configuration.
Options: Auto, 45W, 55W, 85W, 120W.

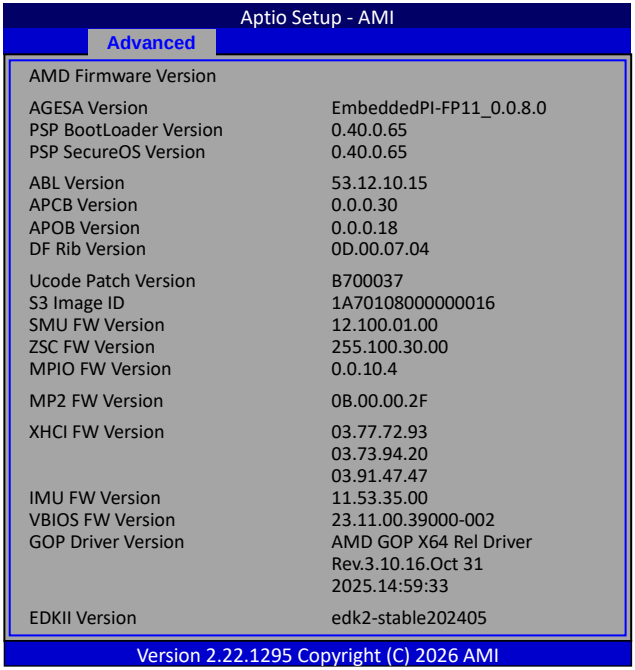
*Warning: Select System Configuration may cause the system to hang, as some System Configuration may not be supported by your OPN.*

## ▶ AMD PBS

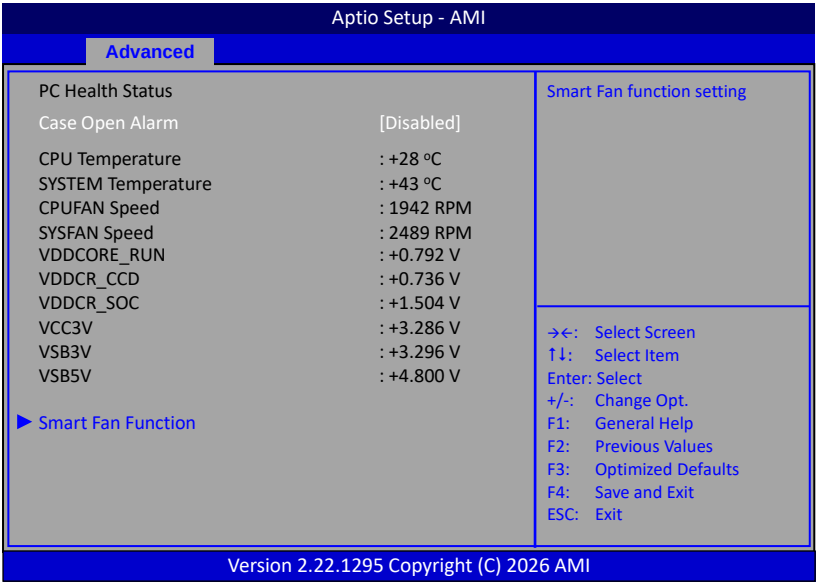



**AMD Firmware Version**

Show all of AMD Firmware Version.

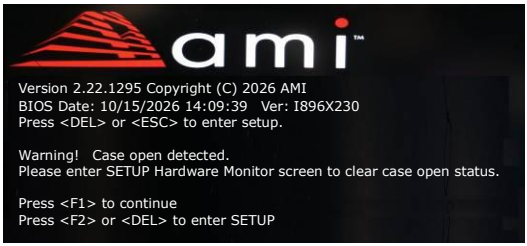


## ▶ Hardware Monitor




**Case Open Alarm**

The chassis intrusion detection alerts you whenever your computer chassis was opened. If the case cover is opened, the system will automatically restart and appear prompt message (Shown below) during POST.




**CPU / SYSTEM Temperature**

Displays the current APU / System temperature.

**CPUFAN Speed / SYSFAN Speed**

Displays the current CPU / System Fan Speeds.

**VDDCORE_RUN / VDDCR_CCD / VDDCR_SOC / VCC3V / VSB3V / VSB5V**

The current voltages are automatically detected and displayed by the system.

## Smart Fan Configuration

### CPUFAN Configuration / SYSFAN Configuration

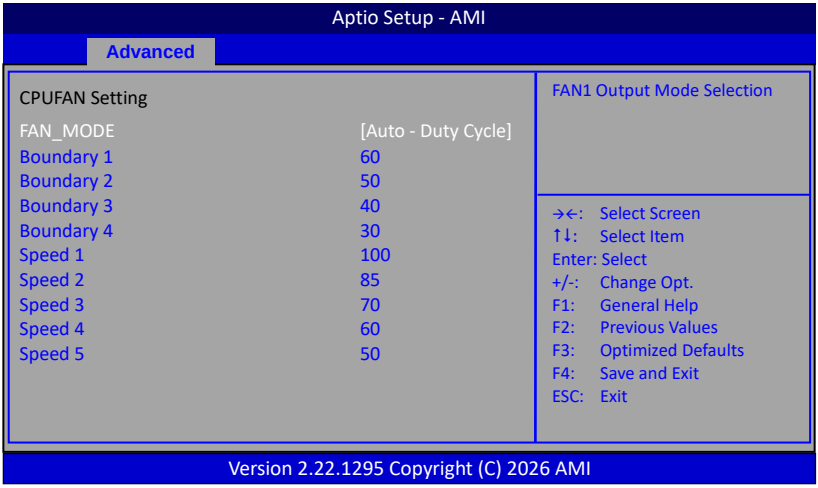
#### CPUFAN MODE / SYSFAN MODE

This field controls the speed of the various fans on the motherboard.

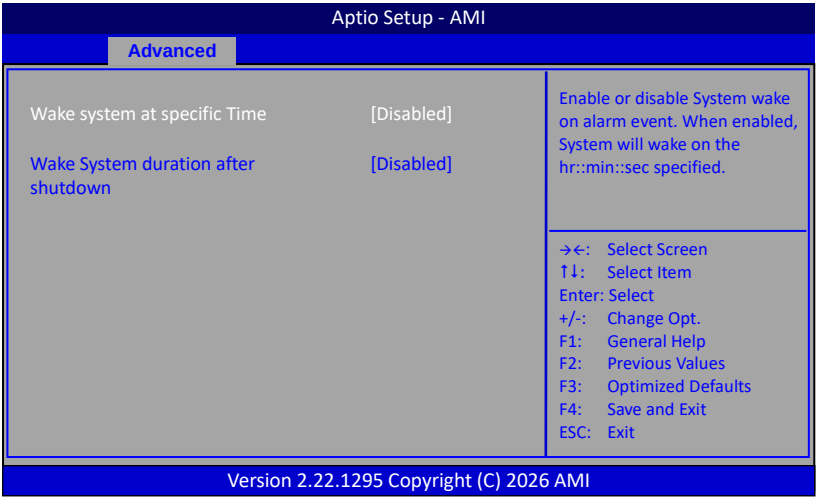
Auto - Duty Cycle: When you want the speed of the fans automatically controlled based on temperature.

Manual - RPM: This item sets the fan speed at a fixed.

Manual - Duty Cycle: To set the fan speed to a constant rate, the speed from 0% to 100%.



## ▶ RTC Wake Settings




**Wake system at specific Time**

Enable or disable system wakeup on alarm event. When enabled, the related items will appear.

Options: Enabled, Disabled.

**Wake up days of the week**

This item allows you to select days of the week to wake up the system.

Options: Every day, Selective.

**Wake up hour / Wake up minute**

This item allows you to set the system to wake up at the hr:min specified.

**Wake System duration after shutdown**

When enabled, system will wake up at current time + Increment in minutes(s) after shutdown. When enabled, the related items will appear.

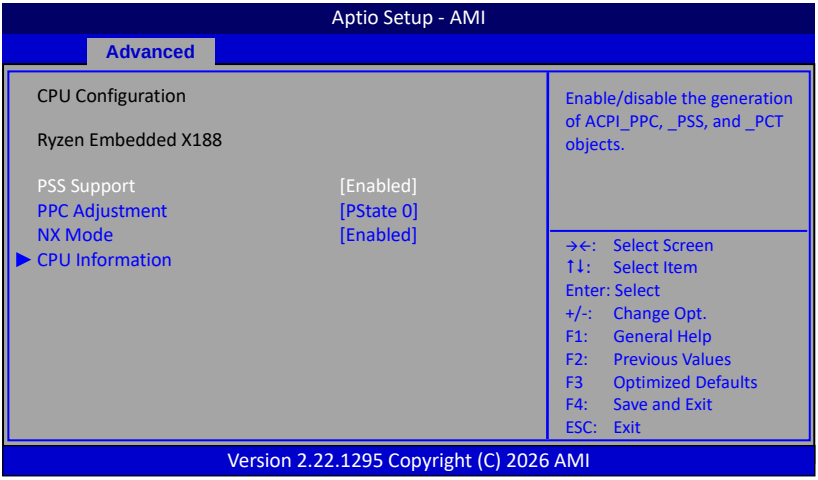
Options: Enabled, Disabled.

**Duration (minute)**

This item allows you to set duration time to wake system.

Options: 1 ~ 30.

## ▶ CPU Configuration




**PSS Support**

Enable/disable the generation of ACPI_PPC, _PSS, and _PCT objects.
Options: Enabled, Disabled.

**PPC Adjustment**

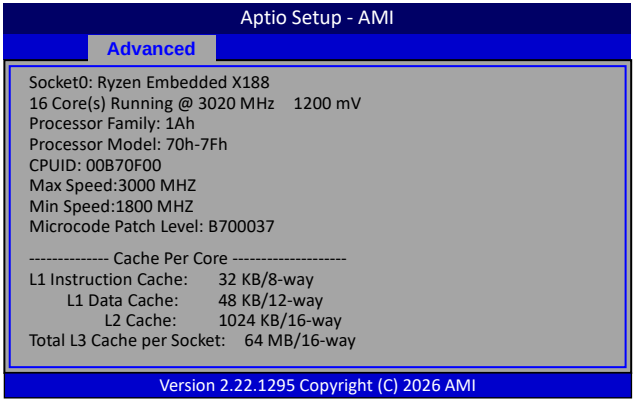
Allows you to adjust _PPC object.
Options: PState 0, PState 1, PState 2.

**NX Mode**

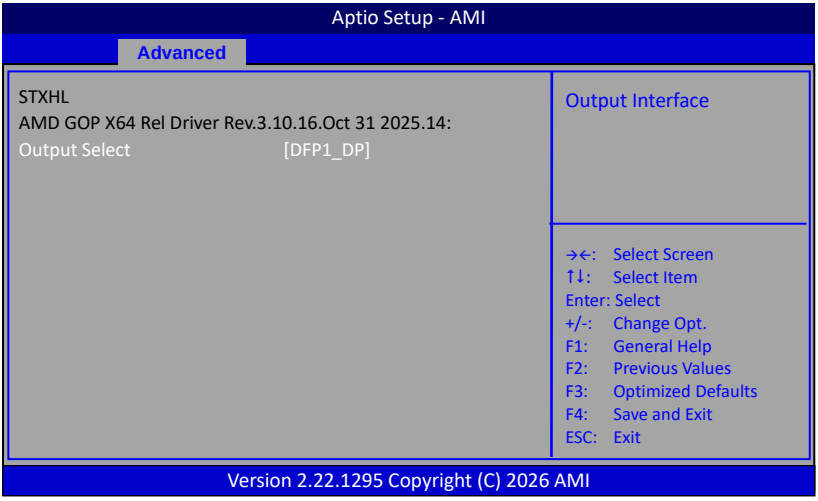
Enable or disable No-execute page protection function.
Options: Enabled, Disabled.

**CPU Information**

Displays current processor information.



## ▶ AMI Graphic Output Protocol Policy

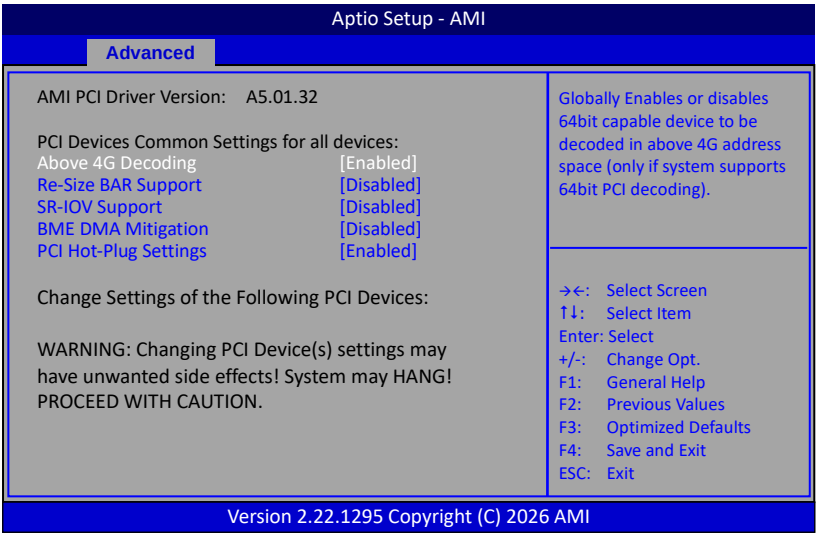



**Output Select**

This item allows you to select the output interface.

Options: DFP1_DP.

## ▶ PCI Subsystem Settings



**Above 4G Decoding**
Enable or disable 64bit capable device to be decoded in above 4G address space (only if system supports 64bit PCI decoding).
Options: Enabled, Disabled.

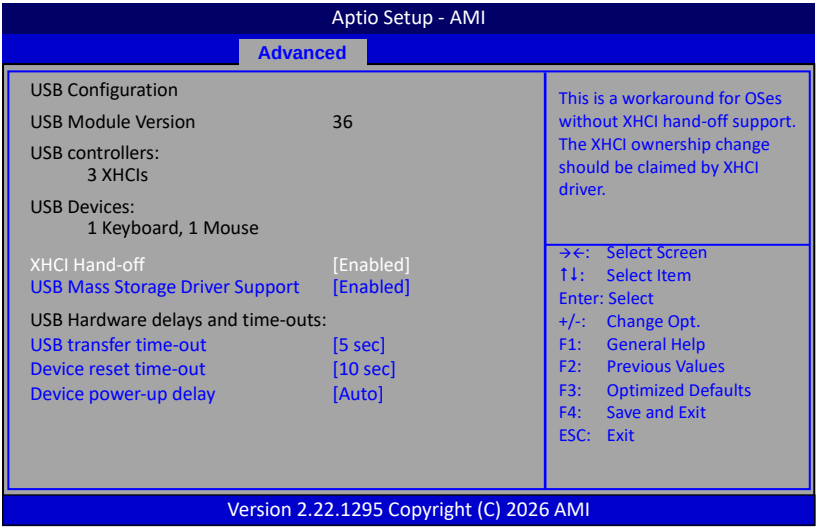
**Re-size BAR Support**
If system has Resizable BAR capable PCIe devices, this option enables or disables Resizable BAR support.
Options: Enabled, Disabled.

**SR-IOV Support**
If system has SR-IOV capable PCIe devices, this option enables or disables Single Root IO Virtualization support.
Options: Enabled, Disabled.

**BME DMA Mitigation**
Re-enable bus master attribute disabled during PCI enumeration for PCI bridges after SMM locked.
Options: Enabled, Disabled.

**Hot-Plug Support**
Globally enables or disables Hot-Plug support for the entire system. If system has Hot-Plug capable slots and this option set to Enabled, it provides a setup screen for selecting PCI resource padding for Hot-Plug.
Options: Enabled, Disabled.

## ▶ USB Configuration




**XHCI Hand-off**

This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.

Options: Enabled, Disabled.

**USB Mass Storage Driver Support**

Allows you to enable or disable USB Mass Storage Driver support.

Options: Enabled, Disabled.

**USB transfer time-out**

The time-out value for control, bulk, and interrupt transfers.

Options: 1 sec, 5 sec, 10 sec, 20 sec.

**Device reset time-out**

Sets USB mass storage devices start unit command time-out.

Options: 10 sec, 20 sec, 30 sec, 40 sec.

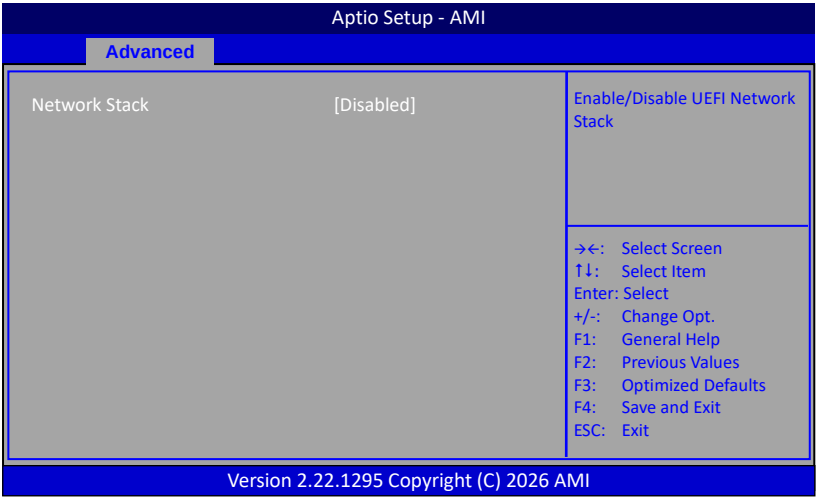
**Device power-up delay**

Maximum time the device will take before it properly reports itself to the Host controller. 'Auto' uses default values: for a Root port it is 100ms, for a Hub port the delay is taken from Hub descriptor.

Options: Auto, Manual.

> **Device power-up delay in seconds**
>
> This item is used to set a wait time in seconds for device power-up delay.
>
> Options: 1 ~ 40.

## ▶ Network Stack Configuration




**Network Stack**

This item is used for network boot in UEFI mode. When enabled, the related items will appear.

Options: Enabled, Disabled.

**Ipv4 PXE Support**

This item is used to enable or disable the Ipv4 PXE boot support. If disabled, Ipv4 PXE boot option will not be available.

Options: Enabled, Disabled.

**Ipv4 HTTP Support**

This item is used to enable or disable the Ipv4 HTTP boot support. If disabled, Ipv4 HTTP boot option will not be available.

Options: Enabled, Disabled.

**Ipv6 PXE Support**

This item is used to enable or disable the Ipv6 PXE boot support. If disabled Ipv6 PXE boot option will not be available.

Options: Enabled, Disabled.

**Ipv6 HTTP Support**

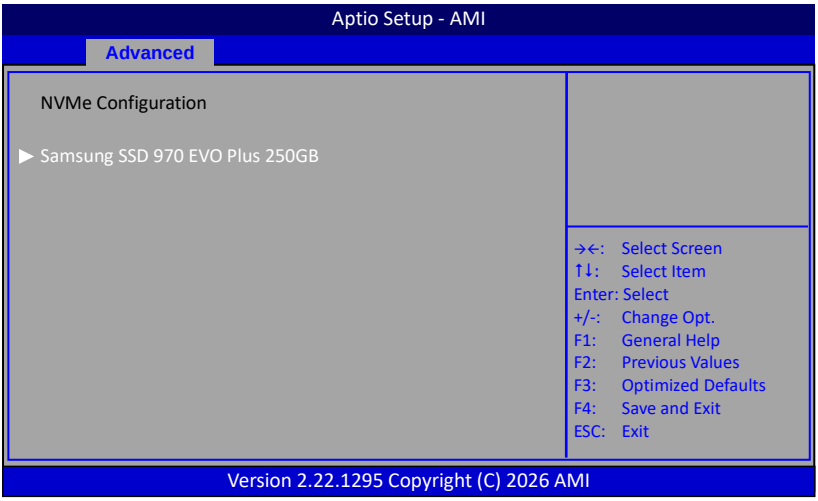
This item is used to enable or disable the Ipv6 HTTP boot support. If disabled, Ipv6 HTTP boot option will not be available.

Options: Enabled, Disabled.

**PXE boot wait time**
This item is used to set a wait time in seconds for PXE boot. Press ESC key to abort the PXE boot.
Options: 0~5 sec.

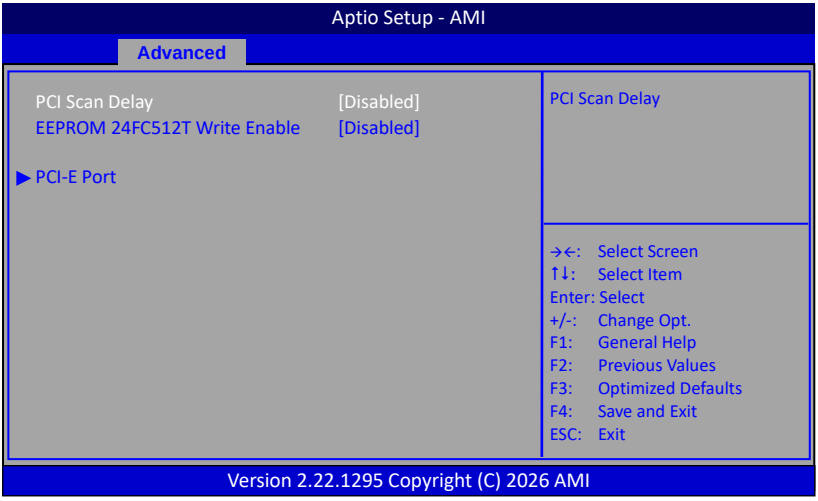
**Media detect count**
Number of times presence of media will be checked.

## ▶ NVMe Configuration




This field is displayed the NVMe controller and Drive information.

## ▶ Onboard Device




**PCI Scan Delay**

Allows you to select a few seconds before detecting expansion board s.
Options: Disabled, Delay 1 seconds, Delay 2 seconds, Delay 3 seconds, Delay 4 seconds, Delay 5 seconds, Delay 10 seconds, Delay 20 seconds, Delay 30 seconds, Delay 40 seconds, Delay 50 seconds, Delay 60 seconds.

**EEPROM 24FC512T Write Enable**

Allows you controls write access to the EEPROM 24FC512T.
Set to Enabled only during firmware flashing or update operations.
Keep Disabled during normal operation to protect data integrity and allow LAN switch IC to function properly.
Options: Disabled, Enabled.

**PCI-E Port**

**PCI-E Port Control**

Allows you to enable or disable the PCIE Port control. If sets to Disabled, skip this page setup item, and use the default CRB setting.
Options: Disabled, Enabled.

**Device 3 Fun 1 (OCulink x4, J15)**

Allows you to enable or disable the OCulink x4 connector.
If sets to Auto, used board default setting.
Options: Disabled, Enabled, Auto.

**Device 3 Fun 2 (Versal VE3558)**
Allows you to enable or disable the AMD Versal AI Edge Gen2 2VE3558.
If sets to Auto, used board default setting.
Options: Disabled, Enabled, Auto.

**Hotplug Mode(Dev#3/Func#2)**
NB Root Hotplug Mode Control.
Options: Disabled, Hotplug Basic, Hotplug Server, Hotplug Enhanced, Hotplug Inboard, Auto.

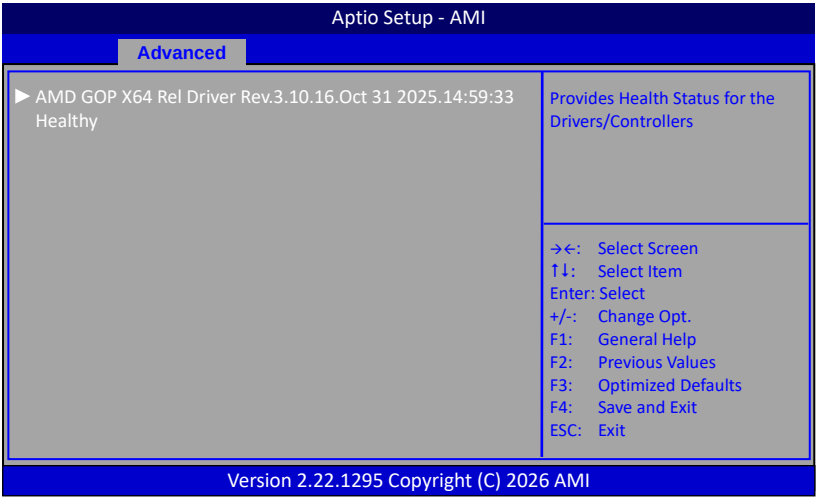
**Device 2 Fun 1 (10G LAN, Bottom)**
Allows you to enable or disable the 10G LAN port (bottom of panel) from LAN AQC113 controller.
If sets to Auto, used board default setting.
Options: Disabled, Enabled, Auto.

**Device 2 Fun 2 (10G LAN, Internal)**
Allows you to enable or disable the LAN AQC113 controller.
If sets to Auto, used board default setting.
Options: Disabled, Enabled, Auto.

**Device 2 Fun 3 (M.2 E-Key, M1)**
Allows you to enable or disable the M.2 E-Key socket.
If sets to Auto, used board default setting.
Options: Disabled, Enabled, Auto.

**Device 2 Fun 4 (M.2 M-Key, M2)**
Allows you to enable or disable the M.2 M-Key socket.
If sets to Auto, used board default setting.
Options: Disabled, Enabled, Auto.

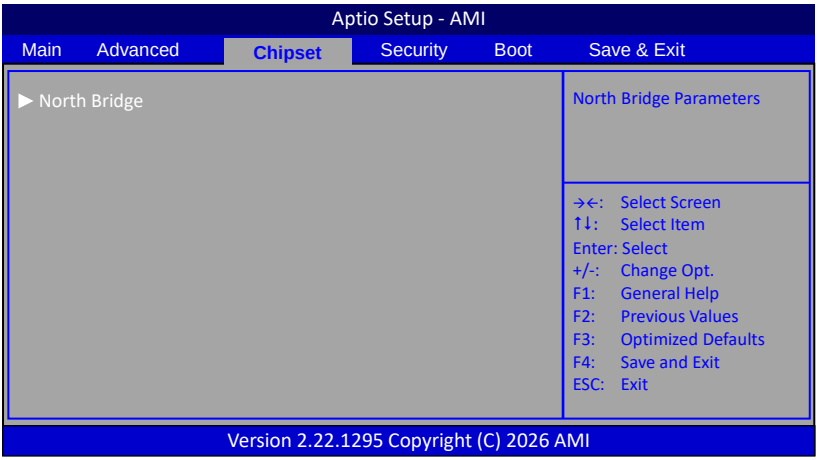
## ▶ Driver Health



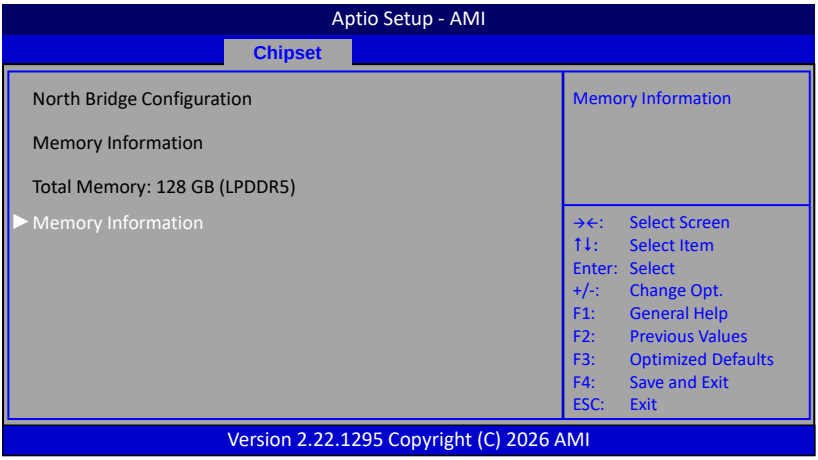

This feature displays the health status for the drivers/controllers.

## *4.5 Chipset Menu*

The chipset menu items allow you to change the advanced chipset settings. Press <Enter> to display the sub-menu.

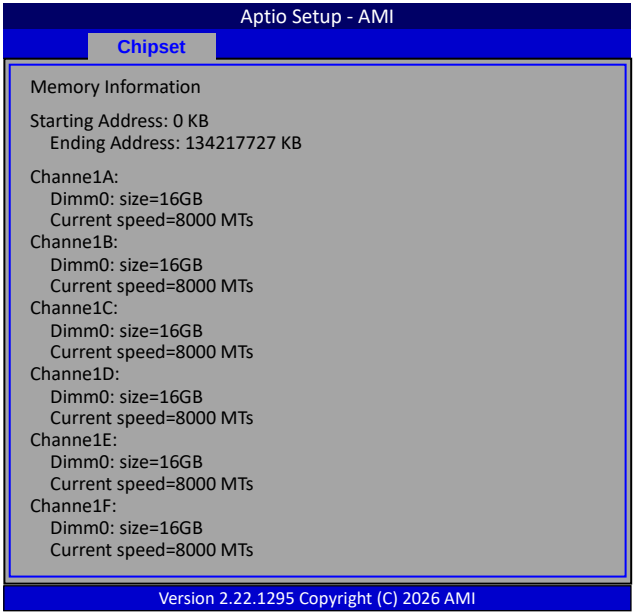



### ▶ North Bridge



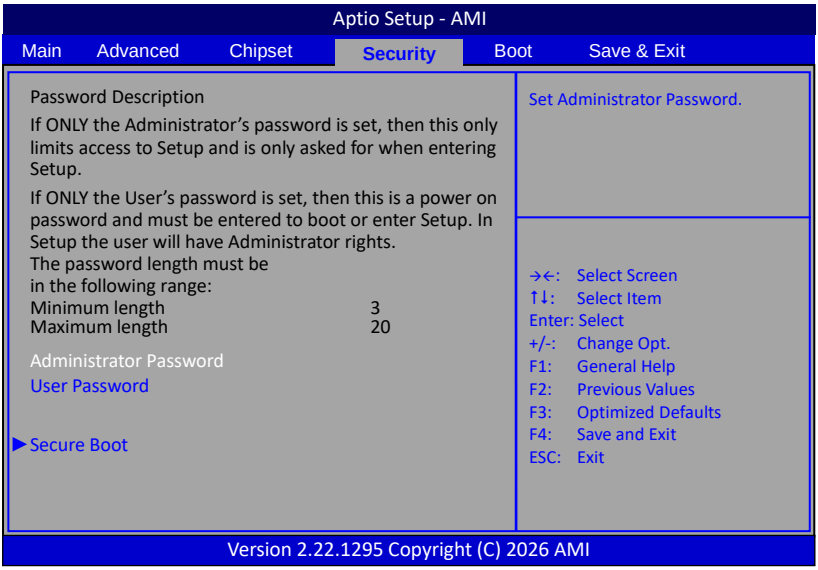
### Memory Information

Displays the memory related information.



## *4.6 Security Menu*

The Security menu allows you to change the system security settings.




**Administrator Password**

This function is used to set, change or delete the Administrator password. If there is already a password installed, the system asks for this first. To clear a password, simply enter nothing and acknowledge by pressing Return. To set a password, enter it twice and acknowledge by pressing Return. The password must be 3 to 20 characters long.

**User Password**

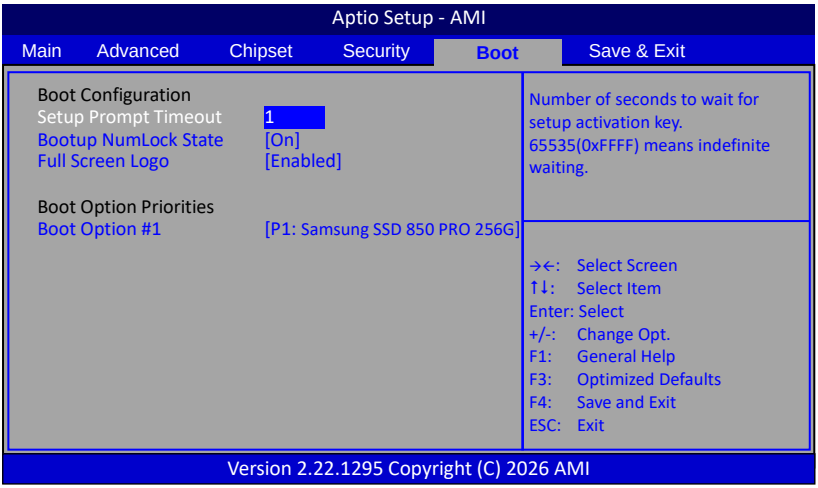
This function is used to set, change or delete the User password. If there is already a password installed, the system asks for this first. To clear a password, simply enter nothing and acknowledge by pressing Return. To set a password, enter it twice and acknowledge by pressing Return. The password must be 3 to 20 characters long.

**Secure Boot**

Secure Boot feature is Active if Secure Boot is Enabled. Platform Key (PK) is enrolled and the system is in user mode. The mode change requires platform reset.

## 4.7 Boot Menu

The Boot menu is used to configure the boot settings and the boot priority.




**Setup Prompt Timeout**

This is used to set an additional time the POST should wait for the operator to press the key to enter setup. The time is entered in seconds.

**Bootup NumLock State**

Selects the state of the keyboard's Numlock function after POST.
Options: On, Off.

**Full Screen Logo**

This item allows you to enable or disable the full screen logo display feature.
Options: Enabled, Disabled.

**Boot Option Priorities**

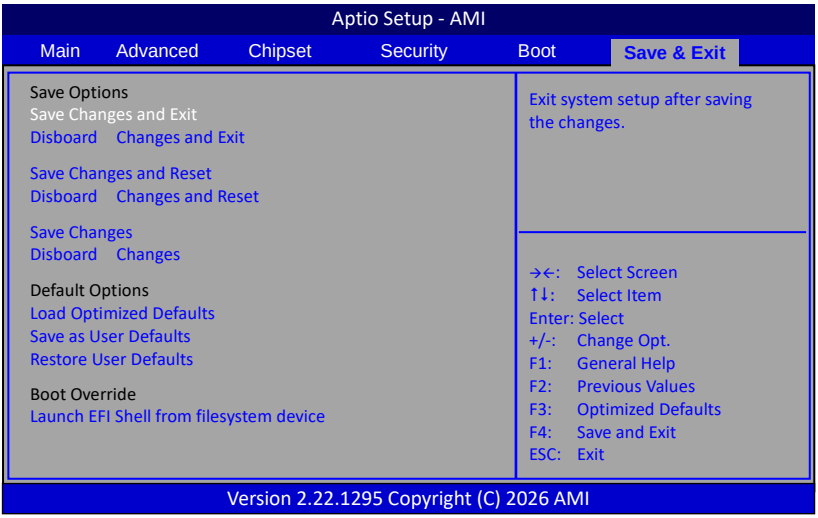
These items specify the boot device priority sequence of the available devices. The number of device items that appears on the screen depends on the number of devices installed in the system.

**Hard Drive BBS Priorities**

Allows you to configure the boot order for a specific Hard Drive device class.

## *4.8 Save & Exit Menu*

The Save & Exit menu allows you to load the optimal default values for BIOS, and save or disboard your changes to the BIOS items.




**Save Changes and Exit**

This exits system after saving the changes.

**Disboard Changes and Exit**

This exits system without saving the changes.

**Save Changes and Reset**

This resets system after saving the changes.

**Disboard Changes and Reset**

This resets system without saving the changes.

**Save Changes**

Allows you to save the changes you made.

**Disboard Changes**

Allows you to disboard the changes you made.

**Load Optimized Defaults**

The load default values are the factory settings of this motherboard.

**Save as User Defaults**

This saves a copy of the current BIOS settings as the user defaults.

**Restore User Defaults**
This restores from your user default.

**Boot Override**
This group of functions includes a list, each of them corresponding to one device within the boot order. Select a drive to immediately boot that device regardless of the current boot order.

**Launch EFI Shell from filesystem device**
Attempts to launch EFI Shell application (Shellx64.efi) form one of the available filesystem devices.