



# User's Manual

**AMD Versal Plus Ryzen Mini-ITX Board  
VPR-4616-MB**

## **TRADEMARK**

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These specifications are subject to change without notice.

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## Federal Communications Commission (FCC) Statement

This device has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with instructions contained in this manual, may cause harmful interference to radio and television communications. However, there is no guarantee that interference will not occur in a particular installation.

If this product does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the product into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

 Note1: Connecting this device to peripheral devices that do not comply with Class B requirements, or using an unshielded peripheral data cable, could also result in harmful interference to radio or television reception.

 Note2: The user is cautioned that any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this product.

 Note3: To ensure that the use of this product does not contribute to interference, it is necessary to use shielded I/O cables.

## CE: Radiation of EN 55022 & Immunity of EN 55024

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## Waste Electrical and Electronic Equipment (WEEE) Statement

To protect the global environment, this product must be sent to separate collection facilities for recovery and recycling.



### DISPOSAL

Do not dispose of this product as unsorted municipal waste. Collect such waste separately for special treatment.



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## Manufacturer

Sapphire Technology Limited  
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# Table of Contents

|                                                            |           |
|------------------------------------------------------------|-----------|
| <b>Chapter 1 Introduction .....</b>                        | <b>1</b>  |
| 1-1 Mainboard Specifications .....                         | 1         |
| 1-2 Package Contents .....                                 | 4         |
| 1-3 Mainboard Layout .....                                 | 5         |
| 1-4 Mainboard Dimension .....                              | 9         |
| <b>Chapter 2 Installation .....</b>                        | <b>11</b> |
| 2-1 Installing System Memory .....                         | 11        |
| Memory Configuration .....                                 | 11        |
| Memory Installation .....                                  | 11        |
| 2-2 Installing Expansion Cards (Additional Purchase) ..... | 12        |
| IO Expansion Board Socket .....                            | 12        |
| Dual Ethernet 1G Card .....                                | 14        |
| GMSL Card .....                                            | 16        |
| M.2 E-Key Slot Installation .....                          | 22        |
| M.2 M-Key Slot Installation .....                          | 23        |
| 2-3 Connecting Cables and Jumper Settings .....            | 26        |
| Front Panel Header .....                                   | 26        |
| SATA Power Header .....                                    | 28        |
| USB2.0 Header .....                                        | 28        |
| COM Header .....                                           | 29        |
| Case Open Header .....                                     | 29        |
| Speaker Header .....                                       | 29        |
| AMD FPGA JTAG Port (Internal Use Only) .....               | 29        |
| AMD APU HDT+ Header (Internal Use Only) .....              | 30        |
| VE2302 GPIO1 Header .....                                  | 30        |
| AMD APU HDT Warm Reset Header (Internal Use Only) .....    | 30        |
| VE2302 GPIO2 Header .....                                  | 30        |
| AMD GPIO Header .....                                      | 31        |
| External USB INPUT Connector (USB2-DEUG) .....             | 31        |
| Fan Headers .....                                          | 31        |
| PSLP Power Control Jumper (JP1) .....                      | 32        |
| PSFP Power Control Jumper (JP2) .....                      | 32        |
| FUSE Power Control Jumper (JP3) .....                      | 32        |
| USB Debug Port Selection Jumper of VE2302 (JP4) .....      | 33        |
| VE2302 MODE Selection Jumper (JP5) .....                   | 33        |
| ROM Write Protect mode Jumper (JP6) .....                  | 34        |

---

|                                                    |           |
|----------------------------------------------------|-----------|
| Versal Power Control Jumper (JP7)                  | 34        |
| Main Power Control Jumper (JP8)                    | 34        |
| Auto Power ON Jumper (JP9)                         | 34        |
| Clear CMOS Jumper (CMOS1)                          | 35        |
| 2-4 System LED Status Indicators                   | 36        |
| 2-5 Minimum connection required to boot            | 36        |
| <b>Chapter 3 Configuring the BIOS</b>              | <b>37</b> |
| 3-1 Select Boot Device                             | 37        |
| 3-2 Enter BIOS Setup                               | 37        |
| 3-3 Main Menu                                      | 39        |
| 3-4 Advanced Menu                                  | 40        |
| Trusted Computing                                  | 40        |
| ACPI Settings                                      | 42        |
| SATA Configuration                                 | 43        |
| Onboard Devices                                    | 43        |
| Hardware Monitor                                   | 46        |
| RTC Wake Settings                                  | 48        |
| Serial Port Console Redirection                    | 49        |
| CPU Configuration                                  | 50        |
| SIO Configuration                                  | 51        |
| PCI Subsystem Settings                             | 52        |
| USB Configuration                                  | 53        |
| Network Stack Configuration                        | 55        |
| CSM Configuration                                  | 56        |
| NVMe Configuration                                 | 57        |
| AMD CBS                                            | 58        |
| AMD PBS                                            | 66        |
| AMD Firmware Version                               | 66        |
| 3-5 Chipset Menu                                   | 67        |
| 3-6 Security Menu                                  | 69        |
| 3-7 Boot Menu                                      | 70        |
| 3-8 Save & Exit Menu                               | 71        |
| <b>Chapter 4 Firmware and Driver Installation</b>  | <b>72</b> |
| <b>Chapter 5 Chassis Installation</b>              | <b>73</b> |
| <b>Appendix A: BIOS Update</b>                     | <b>75</b> |
| <b>Appendix B: Qualified Vendors List</b>          | <b>76</b> |
| <b>Appendix C: Expansion Board &amp; Connector</b> | <b>80</b> |
| <b>Appendix D: VPR-4616-SYS Default Login</b>      | <b>80</b> |

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## Technical Support and Assistance

1. Visit the Sapphire Technology website at <https://support.sapphiretech.com/ticket-choose.asp?PDtype=EMB&lang=eng> to open a support ticket.
2. Contact your distributor, sales representative, or Sapphire's customer service center for technical support if you need additional assistance. Please have the following information ready before calling:
  - Product name and serial number
  - Description of your peripheral attachments
  - Description of your software (operating system, version, application software, etc.)
  - Comprehensive description of the problem
  - The exact wording of any error messages
3. Reference links

Xilinx Wiki - AMD Embedded+ Platform - General description of the AMD Embedded+ platform architectures which captures an AMD x86 paired with an AMD Adaptive SoC.

<https://xilinx-wiki.atlassian.net/wiki/spaces/A/pages/3011838141/AMD+Embedded+Platforms>

AMD Github - Embedded+ HW/PL platform repository.

GitHub - Xilinx/emb\_plus\_vitis\_platforms

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# **Chapter 1 Introduction**

## ***1-1 Mainboard Specifications***

### **APU**

- AMD® R2314 APU for FP5 package with Zen 2 core

### **Graphics**

- AMD® Radeon series graphics
- Supports two independent displays with DisplayPort and HDMI port
  - ※ One DisplayPort supports a maximum resolution of 3840x2160@60Hz/144Hz
    - \* Support for DisplayPort 1.4 version, HDCP 2.3 and HDR
  - ※ One HDMI port supports a maximum resolution of 3840x2160@60Hz/120Hz
    - \* Support for HDMI 2.1 version, HDCP 2.3 and HDR

### **System Memory**

- Two 260-pin DDR4 SDRAM SO-DIMM (ECC/Non ECC) sockets
- Supports 1.2V DDR4-2133/2400/2666 DIMMs with dual channel architecture
- Supports 4GB, 8GB, 16GB and 32GB DDR4 SO-DIMMs up to maximum 64GB

### **Xilinx Subsystem**

- Versal Edge VE2302 in the SFVA784 package
- LPDDR4 8GB memory
- Infineon OPTIGA™ TPM SLM 9670 TPM2.0 in PG-VQFN-32-13 package

### **Expansion Slots**

- One M.2 Slot E-key (PCIe x1 and USB2.0) with 2230 type for Wifi/BT
- One M.2 Slot M-key (PCIe 3.0 x4 and SATA) with 2280/2580 storage type for SSD

### **USB Ports**

- Three USB 2.0 ports (two at rear panel, one onboard headers), supporting transfer speed up to 480Mbps
- Two USB3.1 Gen 2 ports at rear panel supporting transfer speed up to 10Gbps

- 
- One USB3.1 Gen 2 Type C port at back panel supporting transfer speed up to 10Gbps
  - Supports wake-up from S3 and S4 modes

### **SATA Port**

- One SATA3 port with 6Gb/s data transfer rate
- Supports AHCI (Advanced Host Controller Interface)

### **Onboard LAN**

- 2.5 Gigabit Ethernet from Realtek® RTL8125BG Gigabit controller

### **Onboard Audio**

- High-Definition audio from Realtek ALC888S codec

### **I/O**

- Onboard Fintek F81803U LPC bus I/O controller
- Supports Hardware Monitor for fan speed monitoring, CPU and system temperature

### **Back Panel I/O Ports**

- 1 x DC-in 12V~19V Jack
- 1 x DisplayPort
- 1 x HDMI Port
- 2 x USB2.0 ports (Black)
- 2 x USB3.1 Gen 2 ports (Blue)
- 1 x RJ45 2.5 Gigabit LAN port
- 1 x COM port
- 1 x USB3.1 Gen 2 Type C Port
- 1 x Line-Out port
- 1 x Min-In port

### **Internal I/O Connectors**

- 1 x DC-in 4-pin 12V~19V Power Connector (PW1)
- 1 x IO Expansion Board Socket, connect to daughter card (J1)

- 
- 1 x SATA3 Connectors (S1)
  - 1 x SATA Power Header, 1x4pin 2.50mm pitch (SATA\_PW)
  - 1 x USB2.0 Headers, 1x4pin 2.54mm pitch (USB2-A, supports 1 USB2.0 port)
  - 1 x Front Panel Header, 2x5pin 2.54mm pitch (CFP1)
  - 1 x Speaker Header, 1x4pin 2.54mm pitch (CSPK)
  - 1 x COM Headers for RS232/422/485, 2x5pin 2.54mm pitch (COM2)
  - 1 x Battery Headers, 1x2pin 1.25mm pitch (BAT)
  - 1 x AMD FPGA JTAG Port, 2x7pin 2.54mm pitch (J2)
  - 1 x AMD APU HDT+ Header, 2x10pin 1.27mm pitch (J5)
  - 1 x VE2302 GPIO1 Header, 1x2pin 2.54mm pitch (J6)
  - 1 x AMD APU HDT Warm Reset Header, 1x2pin 2.54mm pitch (J7)
  - 1 x VE2302 GPIO2 Header, 1x2pin 2.54mm pitch (J8)
  - 1 x AMD GPIO Header, 2x5pin 2.54mm pitch (J9)
  - 1 x Case Open Header, 1x2pin 2.54mm pitch (J12)
  - 1 x CPU Fan Header, 1x4pin 2.54mm pitch (CPUFAN)
  - 1 x SYSTEM Fan Header, 1x3pin 2.54mm pitch (SYSFAN)
  - 1 x PSLP POWER Control Jumper, 1x3pin 2.54mm pitch (JP1)
  - 1 x PSFP POWER Control Jumper, 1x3pin 2.54mm pitch (JP2)
  - 1 x FUSE Power Control Jumper, 1x3pin 2.54mm pitch (JP3)
  - 1 x USB Debug Port Selection Jumper of VE2302, 1x3pin 2.54mm pitch (JP4)
  - 1 x VE2302 MODE Selection, 1x2pin 2.54mm pitch (JP5)
  - 1 x ROM Write Protect mode Jumper, 1x3pin 2.54mm pitch (JP6)
  - 1 x Versal Power Control Jumper, 1x3pin 2.54mm pitch (JP7)
  - 1 x Main Power Control Jumper, 1x3pin 2.54mm pitch (JP8)
  - 1 x Auto Power ON Jumper, 1x3pin 2.54mm pitch (JP9)
  - 1 x Clear CMOS Jumper, 1x3pin 2.54mm pitch (CMOS1)
  - External USB INPUT Connector For VE2302 debug use (USB2-DEUG)

## **BIOS**

- 64Mb SPI Flash with AMI based BIOS
- Supports ACPI (Advanced Configuration and Power Interface)

- 
- Onboard jumper to clear the CMOS data

**Onboard Button**

- Onboard VE2302 Reset button

**Form Factor**

- Mini ITX form factor of 170mm×170mm

**Operating systems**

- Supports RHEL/CentOS 7.9; RHEL 8.2- 8.6; Ubuntu 22.04

**Environmental**

- Power Requirement: Power adapter of 12V~19V DC OUT, input voltage tolerance +/- 5%
- Operating Temperature: 0°C~50°C (32°F~122°F)
- Storage Temperature: -20°C~80°C (-4°F~176°F)
- Relative Humidity: 10%~90%

***1-2 Package Contents***

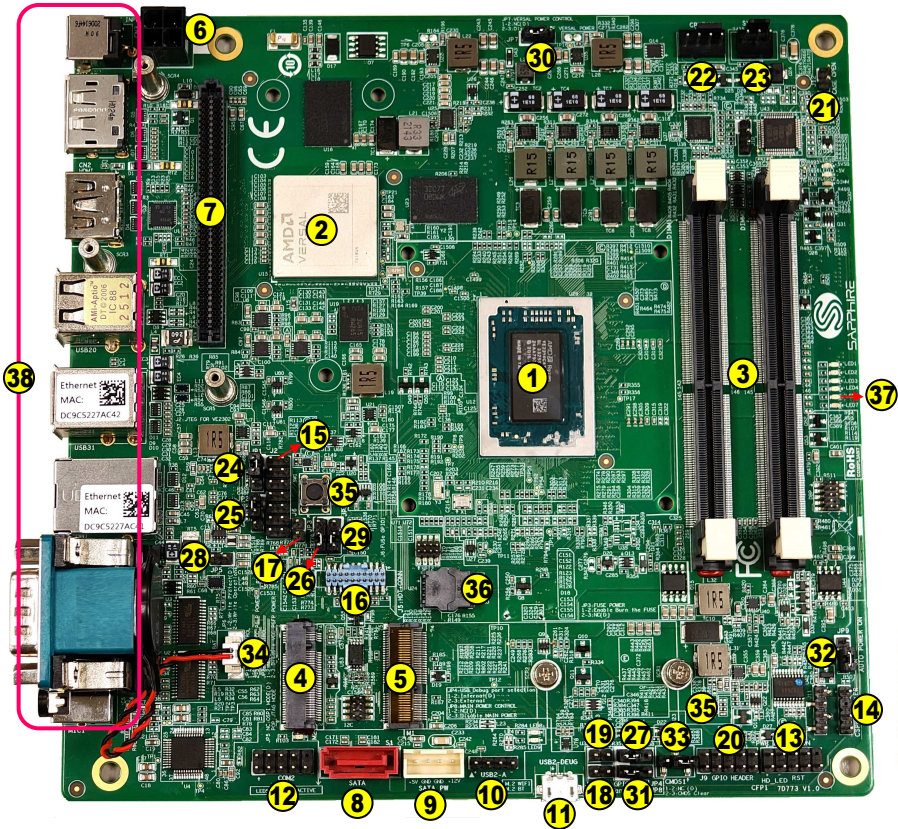
Your mainboard comes with the following items.

| Mainboard x1                                                                        | I/O Shield x1                                                                       |
|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|
|  |  |

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## 1-3 Mainboard Layout

The following figure shows the location of components on the mainboard. See page 6 for component description.



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Note:

Picture is for reference only, actual board may be slightly different.

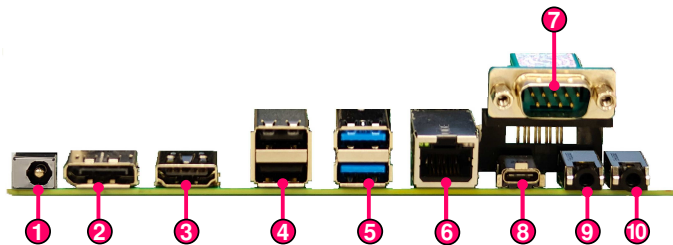
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See next page for details.

| Item | Component description                                          | Location  |
|------|----------------------------------------------------------------|-----------|
| 1    | AMD FP5 APU                                                    | U29       |
| 2    | AMD VE2302 IC                                                  | U15       |
| 3    | DDR4 SO-DIMM *2                                                | DIMM0/1   |
| 4    | M.2 M-key for SSD device                                       | M2        |
| 5    | M.2 E-Key slot for Wifi/BT card                                | M1        |
| 6    | 4-pin 12V~19V Power Connector                                  | PW1       |
| 7    | IO Expansion Board Socket                                      | J1        |
| 8    | SATA3 Connector                                                | S1        |
| 9    | SATA Power Header, 1x4pin 2.50mm pitch                         | SATA_PW   |
| 10   | USB 2.0 Header <sup>(Note)</sup> , 1x4pin 2.54mm pitch         | USB2-A    |
| 11   | External USB INPUT connector for VE2302 debug use              | USB2-DEUG |
| 12   | COM Header for RS232/422/485 mode, 2x5pin 2.54mm pitch         | COM2      |
| 13   | Front Panel Header, 2x5pin 2.54mm pitch                        | CFP1      |
| 14   | Speaker Header, 1x4pin 2.54mm pitch                            | CSPK      |
| 15   | AMD FPGA JTAG Port, 2x7pin 2.54mm pitch                        | J2        |
| 16   | AMD APU HDT+ Header, 2x10pin 1.27mm pitch                      | J5        |
| 17   | VE2302 GPIO1 Header, 1x2pin 2.54mm pitch                       | J6        |
| 18   | AMD APU HDT Warm Reset Header, 1x2pin 2.54mm pitch             | J7        |
| 19   | VE2302 GPIO2 Header, 1x2pin 2.54mm pitch                       | J8        |
| 20   | AMD GPIO Header, 2x5pin 2.54mm pitch                           | J9        |
| 21   | Case Open Header, 1x2pin 2.54mm pitch                          | J12       |
| 22   | CPU Fan header, 1x4pin 2.54mm pitch                            | CPUFAN    |
| 23   | SYSTEM Fan header, 1x3pin 2.54mm pitch                         | SYSFAN    |
| 24   | PSLP POWER Control Jumper, 1x3pin 2.54mm pitch                 | JP1       |
| 25   | PSFP POWER Control Jumper, 1x3pin 2.54mm pitch                 | JP2       |
| 26   | FUSE Power Control Jumper, 1x3pin 2.54mm pitch                 | JP3       |
| 27   | USB Debug Port Selection Jumper of VE2302, 1x3pin 2.54mm pitch | JP4       |
| 28   | VE2302 MODE Selection, 1x2pin 2.54mm pitch                     | JP5       |
| 29   | ROM Write Protect mode Jumper, 1x3pin 2.54mm pitch             | JP6       |
| 30   | Versal Power Control Jumper, 1x3pin 2.54mm pitch               | JP7       |
| 31   | Main Power Control Jumper, 1x3pin 2.54mm pitch                 | JP8       |
| 32   | Auto Power ON Jumper, 1x3pin 2.54mm pitch                      | JP9       |
| 33   | Clear CMOS jumper, 1x3pin 2.54mm pitch                         | CMOS1     |
| 34   | Battery headers, 1x2pin 1.25mm pitch                           | BAT       |
| 35   | VE2302 Reset button                                            | SW1       |
| 36   | BIOS Socket                                                    | U24       |
| 37   | Versal DONE LED                                                | LED6      |
| 38   | Back Panel Connectors (see next page for detail)               |           |

Note: Each USB 2.0 Header can be used to connect 1 USB device.

# I/O Back Panel



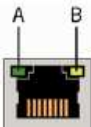
| Item | Description          | Item | Description              |
|------|----------------------|------|--------------------------|
| 1    | DC-IN 12V~19V Jack   | 6    | 2.5G bps RJ45 LAN Port   |
| 2    | Display Port         | 7    | COM Port (RS232/422/485) |
| 3    | HDMI Port            | 8    | USB3.1 Type C Gen 2 Port |
| 4    | USB2.0 Port *2       | 9    | Line-Out port            |
| 5    | USB3.1 Gen 2 Port *2 | 10   | Mic-In port              |

**Note:**  
There are two ways to source power to the board: DC-in jack or 4-pin power connector. Two different physical ports that can only be used one at a time.  
e.g. When DC-in 12V ~ 19V jack is being used, the 4-pin power connector shouldn't be connected to any power source.

**Warning:**  
One of the power inputs may be damaged when connecting both DC jack and 4-pin power connector at the same time.

## LED indicates of LAN Port

Two LEDs are built into the RJ-45 LAN connector. These LEDs indicate the status of the LAN.

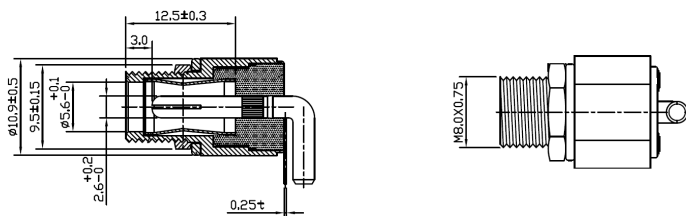


| LED | LED Color | LED state | Indicates                   |
|-----|-----------|-----------|-----------------------------|
| A   | Green     | Off       | LAN link is not established |
|     |           | On        | LAN link is established     |
|     |           | Blinking  | LAN activity is occurring   |
| B   | N/A       | Off       | 10/100M bps data rate       |
|     | Green     | On        | 1000M bps data rate         |
|     | Yellow    | On        | 2.5G bps data rate          |

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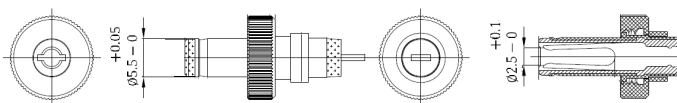
## DC-IN Jack

The DC-IN Jack supports only 12V~19V Input.



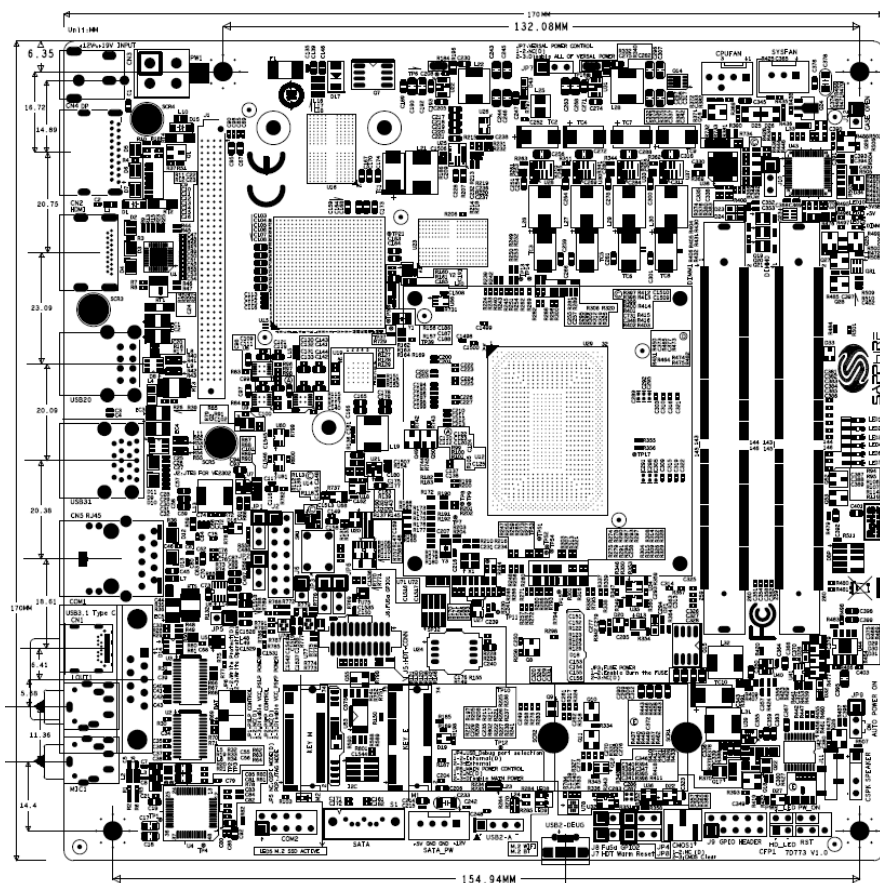
Reference DC power adapter:

- Output Power:  
90W – Without installed PCIe graphic card  
150W – With installed PCIe graphic card
- Output Voltage: 12V~19V



## 1-4 Mainboard Dimension

PCB Size: 170 x 170mm





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# **Chapter 2 Installation**

## ***2-1 Installing System Memory***

This mainboard has two 260-pin SO-DIMM sockets (ECC/Non ECC) for DDR4 memory.

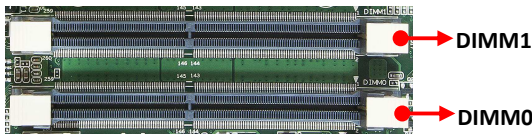
- Supports 4GB, 8GB, 16GB and 32GB DDR4 SO-DIMMs up to maximum 64GB.
- Supports 1.2V DDR4-2133/2400/2666 DIMMs with dual channel architecture.

Make sure that you install memory modules of the same type and density in different channel DIMM slots for Dual-Channel mode.

### **Memory Configuration**

To use 1 DIMM: Install into either DIMM slot 0 or slot 1.

To use 2 DIMMs: Install into DIMM slot 0 and DIMM slot 1.



### **Memory Installation**

DDR4 and DDR3 memory modules are physically different. Please only install DDR4 DIMMs on this mainboard. To make sure you have the correct DIMM, check that all the notches line up with the DDR4 DIMM slot.

To install the DIMM, follow these steps:

1. Pull both clips on either side of the slot outwards. Align the DIMM module with the slot.
2. Press modules straight down until the plastic clips close and the module fits tightly into the DIMM slot. Push clips inwards to make sure they are in place.

To remove DIMM from a socket, gently spread the socket's retention arms to disengage them from the DIMM.

Note: To avoid damaging the DIMM, do not touch its contact edge.

## 2-2 Installing Expansion Cards (Additional Purchase)

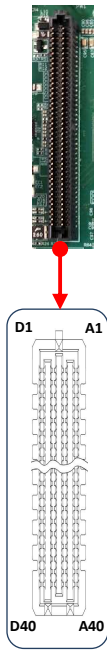
### IO Expansion Board Socket

The mainboard provides one IO Expansion Board Socket, can be used to connect to a daughter card, like Dual Ethernet 1G card and GMSL card etc..

Note: The daughter cards are not included in standard package content. Users may want to purchase the daughter card according to their applications.

J1: IO Expansion Board Socket (Manufacturer PN: SEAF-40-07.5-L-04-1-A-K-TR)

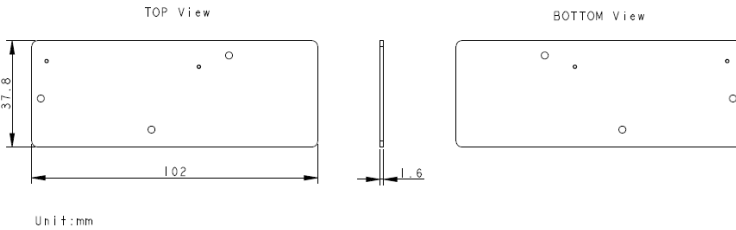
**PIN map between the FPGA and I/O connector on RAVE base board**



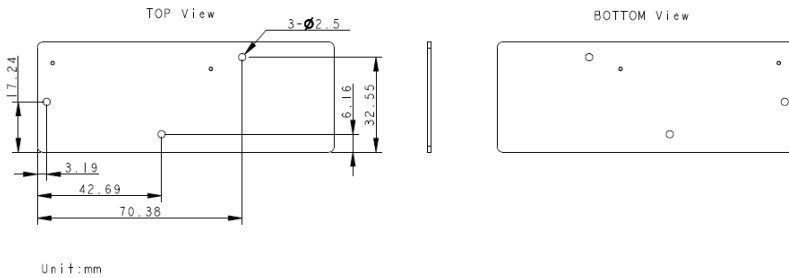
| Conn. Pin | Definition  | FPGA Pin | Conn. Pin | Definition | FPGA Pin | Conn. Pin | Definition    | FPGA Pin | Conn. Pin | Definition      | FPGA Pin |
|-----------|-------------|----------|-----------|------------|----------|-----------|---------------|----------|-----------|-----------------|----------|
| A1        | +3.3V       |          | B1        | +3.3V      |          | C1        | +3.3V         |          | D1        | +3.3V           |          |
| A2        | VCC_CARD_EN | AD6      | B2        | GND        |          | C2        | LPD_MIO4_GPIO | Y2       | D2        | GND             |          |
| A3        | GND         |          | B3        | GTYP_CLKP0 | H7       | C3        | GND           |          | D3        | GTYP_CLKP1      | F7       |
| A4        | GND         |          | B4        | GTYP_CLKN0 | H6       | C4        | GND           |          | D4        | GTYP_CLKN1      | F6       |
| A5        | GND         |          | B5        | GND        |          | C5        | GND           |          | D5        | GND             |          |
| A6        | GTYP_TXP1   | D8       | B6        | GTYP_TXP3  | B8       | C6        | GTYP_TXP2     | C5       | D6        | GTYP_TXP0       | E5       |
| A7        | GTYP_TXN1   | D7       | B7        | GTYP_TXN3  | B7       | C7        | GTYP_TXN2     | C4       | D7        | GTYP_TXN0       | E4       |
| A8        | GND         |          | B8        | GND        |          | C8        | GND           |          | D8        | GND             |          |
| A9        | GTYP_RXP0   | F2       | B9        | GTYP_RXP1  | D2       | C9        | GTYP_RXP2     | B2       | D9        | GTYP_RXP3       | A5       |
| A10       | GTYP_RXN0   | F1       | B10       | GTYP_RXN1  | D1       | C10       | GTYP_RXN2     | B1       | D10       | GTYP_RXN3       | A4       |
| A11       | GND         |          | B11       | GND        |          | C11       | GND           |          | D11       | GND             |          |
| A12       | XPIO_L0P    | J27      | B12       | XPIO_L1P   | H27      | C12       | XPIO_L2P      | G27      | D12       | XPIO_L3P        | E27      |
| A13       | XPIO_L0N    | H28      | B13       | XPIO_L1N   | G28      | C13       | XPIO_L2N      | F28      | D13       | XPIO_L3N        | E28      |
| A14       | GND         |          | B14       | GND        |          | C14       | GND           |          | D14       | GND             |          |
| A15       | XPIO_L4P    | D27      | B15       | XPIO_L5P   | C27      | C15       | XPIO_L6P      | H25      | D15       | XPIO_L7P        | G25      |
| A16       | XPIO_L4N    | C28      | B16       | XPIO_L5N   | B28      | C16       | XPIO_L6N      | J26      | D16       | XPIO_L7N        | G26      |
| A17       | GND         |          | B17       | GND        |          | C17       | GND           |          | D17       | GND             |          |
| A18       | XPIO_L8P    | F26      | B18       | XPIO_L9P   | C25      | C18       | XPIO_L10P     | A25      | D18       | XPIO_L11P       | B26      |
| A19       | XPIO_L8N    | E26      | B19       | XPIO_L9N   | B25      | C19       | XPIO_L10N     | A26      | D19       | XPIO_L11N       | B27      |
| A20       | GND         |          | B20       | GND        |          | C20       | GND           |          | D20       | GND             |          |
| A21       | XPIO_L12P   | H23      | B21       | XPIO_L13P  | F22      | C21       | XPIO_L14P     | E22      | D21       | XPIO_L15P       | D24      |
| A22       | XPIO_L12N   | H24      | B22       | XPIO_L13N  | G23      | C22       | XPIO_L14N     | E23      | D22       | XPIO_L15N       | C24      |
| A23       | GND         |          | B23       | GND        |          | C23       | GND           |          | D23       | GND             |          |
| A24       | XPIO_L16P   | C23      | B24       | XPIO_L17P  | A23      | C24       | XPIO_L18P     | G21      | D24       | XPIO_L19P       | E20      |
| A25       | XPIO_L16N   | B23      | B25       | XPIO_L17N  | A24      | C25       | XPIO_L18N     | H22      | D25       | XPIO_L19N       | F21      |
| A26       | GND         |          | B26       | GND        |          | C26       | GND           |          | D26       | GND             |          |
| A27       | XPIO_L20P   | D20      | B27       | XPIO_L21P  | B20      | C27       | XPIO_L22P     | A20      | D27       | XPIO_L23P       | C22      |
| A28       | XPIO_L20N   | D21      | B28       | XPIO_L21N  | C21      | C28       | XPIO_L22N     | A21      | D28       | XPIO_L23N       | B22      |
| A29       | GND         |          | B29       | GND        |          | C29       | GND           |          | D29       | GND             |          |
| A30       | XPIO_L24P   | F23      | B30       | XPIO_L25P  | E24      | C30       | XPIO_L26P     | D25      | D30       | VCCO_XPIO POWER |          |
| A31       | XPIO_L24N   | F24      | B31       | XPIO_L25N  | F25      | C31       | XPIO_L26N     | D26      | D31       | VCCO_XPIO POWER |          |
| A32       | GND         |          | B32       | GND        |          | C32       | GND           |          | D32       | GND             |          |
| A33       | HDIO0       | F14      | B33       | HDIO1      | E14      | C33       | HDIO2         | C14      | D33       | HDIO3           | C13      |
| A34       | HDIO4       | E13      | B34       | HDIO5      | D14      | C34       | HDIO6         | D12      | D34       | HDIO7           | D12      |
| A35       | HDIO8       | F11      | B35       | HDIO9      | E11      | C35       | HDIO10        | D11      | D35       | HDIO11          | C12      |
| A36       | GND         |          | B36       | GND        |          | C36       | GND           |          | D36       | GND             |          |
| A37       | HDIO12      | D10      | B37       | HDIO13     | C10      | C37       | HDIO14        | B10      | D37       | HDIO15          | A10      |
| A38       | HDIO16      | B11      | B38       | HDIO17     | A11      | C38       | HDIO18        | B12      | D38       | VCCO_HDIO POWER |          |
| A39       | HDIO19      | A13      | B39       | HDIO20     | B13      | C39       | HDIO21        | A14      | D39       | VCCO_HDIO POWER |          |
| A40       | GND         |          | B40       | GND        |          | C40       | GND           |          | D40       | GND             |          |

## Expansion Board Dimension Specification

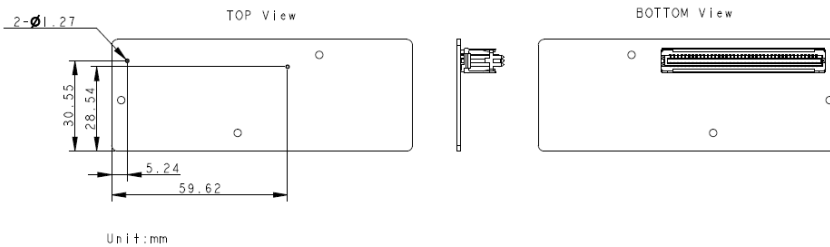
### ● Expansion Board Outline Dimension



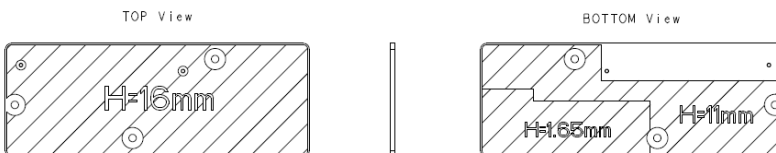
### ● Screw Hole Location & Dimension



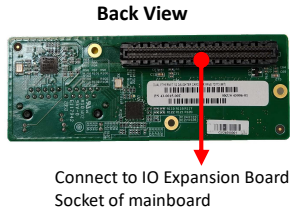
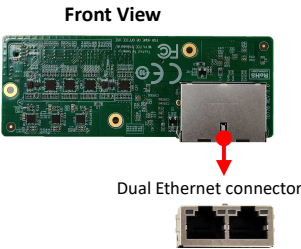
### ● Connector Layout Location SEAM-40-11.0-L-04-2-A-K-TR



### ● Component Height Limit



# Dual Ethernet 1G Card



The RJ45 connector has two indicator LEDs that display the network status:

| RJ45 connector    | LED Position         | Color  | Function                                                                                            |
|-------------------|----------------------|--------|-----------------------------------------------------------------------------------------------------|
| <p>Left Right</p> | Left (Link LED)      | Green  | Lights up when a valid network link is established, indicating a stable connection.                 |
|                   | Right (Activity LED) | Yellow | Lights up when a network link is established and blinks when data is being transmitted or received. |

## Usage Instructions

- The left green LED should remain ON when the device is properly connected to the network, indicating a valid link.
- The right yellow LED will blink when there is network activity, indicating data transmission or reception.
- If the green LED is OFF, check the network cable connection or ensure that the connected device is powered on and functioning properly.
- If the yellow LED does not blink, there may be no active network traffic. Try testing the network connection.

These indicator LEDs help users quickly assess network status and ensure proper device operation!

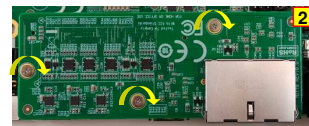
## IO Expansion connector pin map

| Pin # | I/O Bank    | PHY # | PHY Signals | Pin # | I/O Bank  | PHY # | PHY Signals |
|-------|-------------|-------|-------------|-------|-----------|-------|-------------|
| A01   | +3.3V_RUN   |       | 3.3V        | B01   | +3.3V_RUN |       | 3.3V        |
| A02   | VCC_CARD_EN |       | POWER_EN    | B15   | XPIO_L5P  | 0     | ETH_RESET   |
| A15   | XPIO_L4N    | 0     | MDIO        | B16   | XPIO_L5N  | 0     | MDC         |
| A18   | XPIO_L8P    | 0     | TXD2        | B18   | XPIO_L9P  | 0     | RX_CLK      |
| A19   | XPIO_L8N    | 0     | TXD3        | B19   | XPIO_L9N  | 0     | RX_CTL      |
| A21   | XPIO_L12P   | 1     | TX_CLK      | B21   | XPIO_L13P | 1     | TXD0        |
| A22   | XPIO_L12N   | 1     | TX_CTL      | B22   | XPIO_L13N | 1     | TXD1        |
| A30   | XPIO_L24P   | 1     | RX_CLK      | B30   | XPIO_L25P | 1     | RXD1        |
| A31   | XPIO_L24N   | 1     | RX_CTL      | B31   | XPIO_L25N | 1     | RXD0        |
| A37   | HDIO12      | 1     | CLKIN       |       |           |       |             |

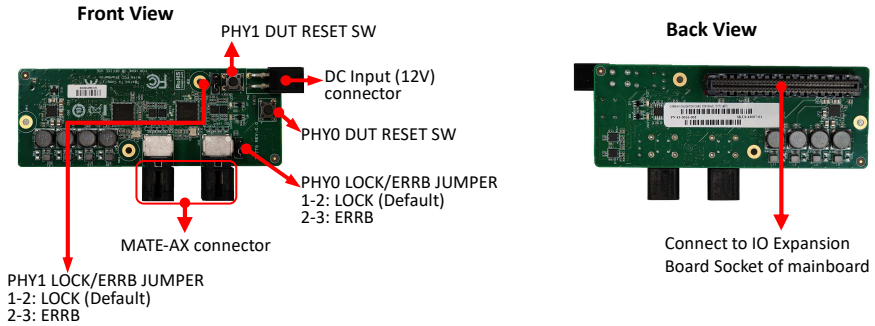
| Pin # | I/O Bank      | PHY # | PHY Signals | Pin # | I/O Bank  | PHY # | PHY Signals |
|-------|---------------|-------|-------------|-------|-----------|-------|-------------|
| C01   | +3.3V_RUN     |       | 3.3V        | D01   | +3.3V_RUN |       | 3.3V        |
| C02   | LPD_MIO4_GPIO |       | Serial I/O  | D15   | XPIO_L7P  | 0     | TXD0        |
| C15   | XPIO_L6P      | 0     | TX_CLK      | D16   | XPIO_L7N  | 0     | TXD1        |
| C16   | XPIO_L6N      | 0     | TX_CTL      | D18   | XPIO_L11P | 0     | RXD2        |
| C18   | XPIO_L10P     | 0     | RXD0        | D19   | XPIO_L11N | 0     | RXD3        |
| C19   | XPIO_L10N     | 0     | RXD1        | D27   | XPIO_L23P | 1     | ETH_RESET   |
| C21   | XPIO_L14P     | 1     | TXD2        | D30   | VCCO_XPIO |       | 1.5V        |
| C22   | XPIO_L14N     | 1     | TXD3        | D31   | VCCO_XPIO |       | 1.5V        |
| C27   | XPIO_L22P     | 1     | MDIO        | D38   | VCCO_HDIO |       | 1.8V        |
| C28   | XPIO_L22N     | 1     | MDC         | D39   | VCCO_HDIO |       | 1.8V        |
| C30   | XPIO_L26P     | 1     | RXD3        |       |           |       |             |
| C31   | XPIO_L26N     | 1     | RXD2        |       |           |       |             |
| C35   | HDIO10        | 0     | CLKIN       |       |           |       |             |

To install the Dual Ethernet 1G Card:

1. Align the card with the IO Expansion Board Socket, and press down on the card until it is completely seated in the slot.
2. Fasten Dual Ethernet 1G Card onto the nut with accompanied screws.



## GMSL Card



CN1 MATE-AX conn. power controller I2C address: 0x50/0x51  
 PHY0 CFG0 controller I2C address: 0x52/0x53  
 PHY0 CFG1 controller I2C address: 0x56/0x57

CN2 MATE-AX conn. power controller I2C address: 0x52/0x53  
 PHY1 CFG0 controller I2C address: 0x50/0x51  
 PHY1 CFG1 controller I2C address: 0x54/0x55

Note: When the value has been adjusted using I2C address.  
 You need to restart the power with A02 pin (POWER\_EN).

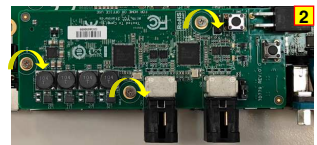
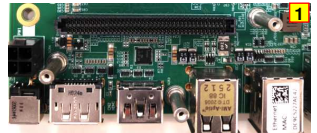
### IO Expansion connector pin map

| Pin # | I/O Bank    | PHY #     | PHY Signals  | Pin # | I/O Bank  | PHY #     | PHY Signals  |
|-------|-------------|-----------|--------------|-------|-----------|-----------|--------------|
| A01   | +3.3V_RUN   |           | 3.3V         | B01   | +3.3V_RUN |           | 3.3V         |
| A02   | VCC_CARD_EN |           | POWER_EN     | B12   | XPIO_L3P  | 1         | DA2P         |
| A15   | XPIO_L2P    | 1         | DA1P         | B13   | XPIO_L3N  | 1         | DA2N         |
| A16   | XPIO_L2N    | 1         | DA1N         | B15   | XPIO_L4P  | 1         | DA0P         |
| A18   | XPIO_L7P    | 0         | DB1P         | B16   | XPIO_L4N  | 1         | DA0N         |
| A19   | XPIO_L7N    | 0         | DB1N         | B18   | XPIO_L8P  | 0         | DB2P         |
| A21   | XPIO_L16P   | 1         | CKBP         | B19   | XPIO_L8N  | 0         | DB2N         |
| A22   | XPIO_L16N   | 1         | CKBN         | B21   | XPIO_L12P | 1         | DB0P         |
| A24   | XPIO_L15P   | 1         | DB3P         | B22   | XPIO_L12N | 1         | DB0N         |
| A25   | XPIO_L15N   | 1         | DB3N         | B27   | XPIO_L21P | 0         | DA0P         |
| A27   | XPIO_L20P   | 0         | DA2P         | B28   | XPIO_L21N | 0         | DA0N         |
| A28   | XPIO_L20N   | 0         | DA2N         | B33   | HDIO1     | Shared    | CFG_I2C_SDA  |
| A33   | HDIO0       | Shared    | CFG_I2C_SCL  | B34   | HDIO5     | PHY0_MFP5 | PHY0_ERRB    |
| A34   | HDIO4       | PHY0_MFP4 | PHY0_LOCK    | B35   | HDIO9     | PHY0_MFP3 | PHY0_GPIO3   |
| A35   | HDIO8       | PHY0_MFP2 | PHY0_GPIO2   | B37   | HDIO13    | PHY1_MFP7 | PT_I2C_SDA_1 |
| A37   | HDIO12      | PHY1_MFP8 | PT_I2C_SCL_1 | B38   | HDIO17    | PHY1_MFP1 | PHY1_GPIO1   |
| A38   | HDIO16      | PHY1_MFP0 | PHY1_GPIO0   | B39   | HDIO20    | PHY0/PHY1 | CFG2_SELO    |
| A39   | HDIO19      | PHY1_MFP3 | PHY1_GPIO3   |       |           |           |              |

| Pin # | I/O Bank      | PHY #      | PHY Signals  | Pin # | I/O Bank  | PHY #      | PHY Signals  |
|-------|---------------|------------|--------------|-------|-----------|------------|--------------|
| C01   | +3.3V_RUN     |            | 3.3V         | D01   | +3.3V_RUN |            | 3.3V         |
| C02   | LPD_MIO4_GPIO |            | Serial I/O   | D12   | XPIO_L5P  | 1          | CKAP         |
| C12   | XPIO_L1P      | 1          | DA3P         | D13   | XPIO_L5N  | 1          | CKAN         |
| C13   | XPIO_L1N      | 1          | DA3N         | D15   | XPIO_L6P  | 0          | DB0P         |
| C15   | XPIO_L10P     | 0          | CKBP         | D16   | XPIO_L6N  | 0          | DB0N         |
| C16   | XPIO_L10N     | 0          | CKBN         | D21   | XPIO_L14P | 1          | DB2P         |
| C18   | XPIO_L9P      | 0          | DB3P         | D22   | XPIO_L14N | 1          | DB2N         |
| C19   | XPIO_L9N      | 0          | DB3N         | D24   | XPIO_L19P | 0          | DA3P         |
| C21   | XPIO_L13P     | 1          | DB1P         | D25   | XPIO_L19N | 0          | DA3N         |
| C22   | XPIO_L13N     | 1          | DB1N         | D30   | VCCO_XPIO |            | 1.2V         |
| C24   | XPIO_L18P     | 0          | CKAP         | D31   | VCCO_XPIO |            | 1.2V         |
| C25   | XPIO_L18N     | 0          | CKAN         | D33   | HDIO3     | PHY0_MFP7  | PT_I2C_SDA_0 |
| C27   | XPIO_L22P     | 0          | DA1P         | D34   | HDIO7     | PHY0_MFP1  | PHY0_GPIO1   |
| C28   | XPIO_L22N     | 0          | DA1N         | D35   | HDIO11    | PHY1_PWDNB | PWDNB_1      |
| C33   | HDIO2         | PHY0_MFP8  | PT_I2C_SCL_0 | D37   | HDIO15    | PHY1_MFP5  | PHY1_ERRB    |
| C34   | HDIO6         | PHY0_MFP0  | PHY0_GPIO0   | D38   | VCCO_HDIO |            | 1.8V         |
| C35   | HDIO10        | PHY0_PWDNB | PWDNB_0      | D39   | VCCO_HDIO |            | 1.8V         |
| C37   | HDIO14        | PHY1_MFP4  | PHY1_LOCK    |       |           |            |              |
| C38   | HDIO18        | PHY1_MFP2  | PHY1_GPIO2   |       |           |            |              |
| C39   | HDIO21        | PHY0/PHY1  | CFG2_SEL1    |       |           |            |              |

To install the GMSL Card:

1. Align the card with the IO Expansion Board Socket, and press down on the card until it is completely seated in the slot.
2. Fasten GMSL Card onto the nut with accompanied screws.



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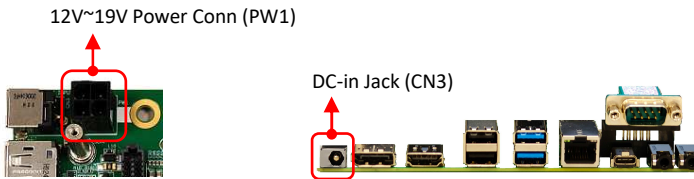
## **PW1 Power Usage:**

PW1 can serve as the power input for the VPR platform, as an alternative to the rear panel DC jack (CN3).

Please note that only one power input — either PW1 or CN3 — should be used at a time. Do not connect power to both simultaneously.

When using an expansion daughtercard that requires a 12V power supply (such as the GMSL daughtercard) and planning to distribute power internally through PW1, please follow the configuration below:

- Use CN3 (DC jack) as the sole power input.
- Use an external power supply that outputs 12V.
  - Although the mainboard supports an input voltage range of approximately 12V to 19V, the daughtercard requires a fixed 12V input voltage.



### **Caution:**

When using the GMSL daughtercard, do not apply an input voltage higher than 12V to avoid damage to the daughtercard.

If supplying power through PW1, please ensure that the voltage requirements of any other connected daughtercards are compatible with the main power input.

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### **Verified GMSL:**

logiCAM-GMSL2-AR0231-05525FM 2.3MP HDR Automotive Video Camera - Narrow Angle Lens

logiCAM-GMSL2-AR0231-DSL182B 2.3MP HDR Automotive Video Camera - Wide Angle Lens

Firmware version : v1.0.1 1\_220323\_1.

Reference Link:

<https://xylon-lab.com/product-category/related-products/gmsl2-cameras/>

Note: The cable which Xylon camera bundles is not compatible with our GMSL2 board.



### **Compatible Quad FAKRA GMSL Cable**

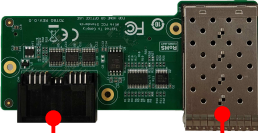
Compatible cables with TE connector (part number : CON-MATE-AX-13\_5H).

Reference Link:

<https://www.wdlsystems.com/CTI-Quad-FAKRA-GMSL-Cable>

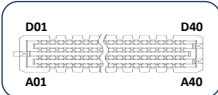
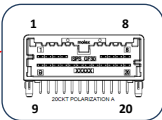
Dual 10/25Gb SFP28 Card

Front View

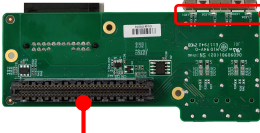


Mini50 connector      SFP28 connector

Mini50 P/N: 34826-8200



Back View



LED1~LED4

LED1: SFP0\_ACT\_LED  
LED2: SFP0\_RX\_LOS\_LED  
LED3: SFP1\_ACT\_LED  
LED4: SFP1\_RX\_LOS\_LED

Connect to IO Expansion Board Socket of mainboard

| Pin | Definition | FPGA Pin | Pin | Definition | FPGA Pin |
|-----|------------|----------|-----|------------|----------|
| 1   | GPI0       | F14      | 9   | GP00       | C13      |
| 2   | GPI1       | E14      | 10  | GP01       | E13      |
| 3   | GPI2       | C14      | 11  | GP02       | D14      |
| 4   | GND        |          | 12  | GPI3       | E12      |
| 5   | GND        |          | 13  | GPI4       | D12      |
| 6   | GPI6       | D10      | 14  | GPI5       | F11      |
| 7   | GPI7       | C10      | 15  | GP03       | E11      |
| 8   | GPI8       | B10      | 16  | GP04       | D11      |
|     |            |          | 17  | GP05       | C12      |
|     |            |          | 18  | GP08       | B12      |
|     |            |          | 19  | GP07       | A11      |
|     |            |          | 20  | GP06       | A10      |

IO Expansion connector pin map

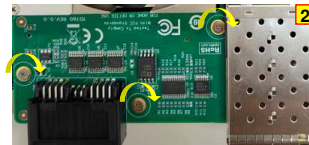
| Connector Pin # | Signals   | FPGA Pin# | Host Signals | Connector Pin # | Signals            | FPGA Pin# | Host Signals   |
|-----------------|-----------|-----------|--------------|-----------------|--------------------|-----------|----------------|
| A01             | +3.3V_RUN |           | +3.3V        | B01             | +3.3V_RUN          |           | +3.3V          |
| A02             | POWER_EN  | AD6       | VCC_CARD_EN  | B03             | REF_CLK0_P         | H7        | GTYP_REFCLK0_P |
| A06             | SFP1_TX_P | D8        | GTYP_TX1_P   | B04             | REF_CLK0_N         | H6        | GTYP_REFCLK0_N |
| A07             | SFP1_TX_N | D7        | GTYP_TX1_N   | B09             | SFP1_RX_P          | D2        | GTYP_RX1_P     |
| A09             | SFP0_RX_P | F2        | GTYP_RX0_P   | B10             | SFP1_RX_N          | D1        | GTYP_RX1_N     |
| A10             | SFP0_RX_N | F1        | GTYP_RX0_N   | B33             | GPI1               | E14       | HDIO1          |
| A33             | GPI0      | F14       | HDIO0        | B34             | GP02               | D14       | HDIO5          |
| A34             | GP01      | E13       | HDIO4        | B35             | GP03               | E11       | HDIO9          |
| A35             | GPI5      | F11       | HDIO8        | B37             | GPI7               | C10       | HDIO13         |
| A37             | GPI6      | D10       | HDIO12       | B38             | GP07               | A11       | HDIO17         |
| A38             | I2C_SCL   | B11       | HDIO16       | B39             | REF_CLK0_DISABLE_L | B13       | HDIO20         |
| A39             | I2C_SDA   | A13       | HDIO19       |                 |                    |           |                |

| Connector Pin # | Signals            | FPGA Pin# | Host Signals  | Connector Pin # | Signals    | FPGA Pin# | Host Signals   |
|-----------------|--------------------|-----------|---------------|-----------------|------------|-----------|----------------|
| C01             | +3.3V_RUN          |           | +3.3V         | D01             | +3.3V_RUN  |           | +3.3V          |
| C02             | Serial I/O         | Y2        | LPD_MIO4_GPIO | D03             | REF_CLK1_P | F7        | GTYP_REFCLK1_P |
| C33             | GPI2               | C14       | HDIO2         | D04             | REF_CLK1_N | F6        | GTYP_REFCLK1_N |
| C34             | GPI3               | E12       | HDIO6         | D06             | SFP0_TX_P  | E5        | GTYP_TX0_P     |
| C35             | GP04               | D11       | HDIO10        | D07             | SFP0_TX_N  | E4        | GTYP_TX0_N     |
| C37             | GPI8               | B10       | HDIO14        | D33             | GP00       | C13       | HDIO3          |
| C38             | GP08               | B12       | HDIO18        | D34             | GPI4       | D12       | HDIO7          |
| C39             | REF_CLK1_DISABLE_L | A14       | HDIO21        | D35             | GP05       | C12       | HDIO11         |
|                 |                    |           |               | D37             | GP06       | A10       | HDIO15         |
|                 |                    |           |               | D38             | VCCO_HDIO  |           | +3.3V          |
|                 |                    |           |               | D39             | VCCO_HDIO  |           | +3.3V          |

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To install the SFP28 Card:

1. Align the card with the IO Expansion Board Socket, and press down on the card until it is completely seated in the slot.
2. Fasten SFP28 Card onto the nut with accompanied screws.

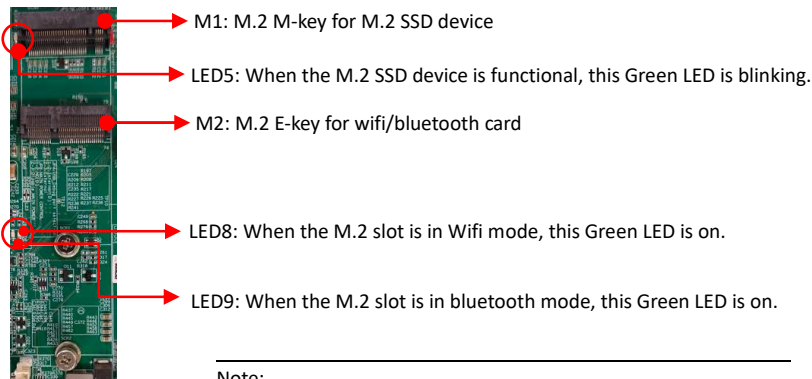


## M.2 E-Key Slot/ M.2 M-Key Slot

The mainboard provides

One M.2 Slot M-key (PCIe 3.0 x4 and SATA) with 2280/2580 storage type for SSD

One M.2 Slot E-key (PCIe x1 and USB2.0) with 2230 type for Wifi/BT



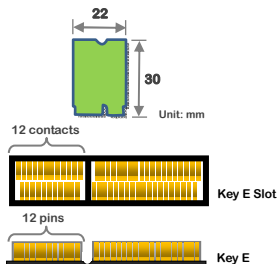
Note:

Recommended torque for the M.2 hold down screws: 1 ~ 1.5lbf.

## M.2 E-Key Slot Installation

To install the M.2 wifi/bluetooth card (type 2230):

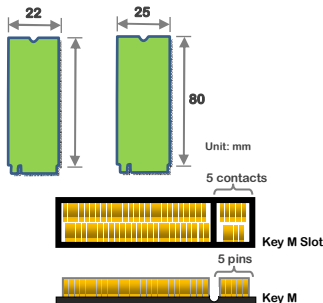
1. Remove screws and align the notch on the M.2 wifi/bluetooth card edge connector with the tab in the slot.
2. Plug the M.2 wifi/bluetooth card firmly into the slot at a 20-degree angle, and until it clicks into place.
3. Fasten M.2 wifi/bluetooth card onto the nut with accompanied screws.



## M.2 M-Key Slot Installation

To install the M.2 SSD device (type 2280/2580):

3. Remove screws and align the notch on the M.2 SSD device edge connector with the tab in the slot.
4. Plug the M.2 SSD device firmly into the slot at a 20-degree angle, and until it clicks into place.
5. Fasten M.2 SSD device onto the nut with accompanied screws.



Note:

The mainboard in the picture is not actual mainboard, just for reference.

## Removing Device Caution

- Remove the M.2 wifi/bluetooth card or M.2 SSD device at a 20-degree angle.
- Please DO NOT pull up the M.2 wifi/bluetooth card or M.2 SSD device to avoid damage to the M.2 slot.



## M.2 E-key 2230 – Supports PCIe x1 & USB2.0 based device

| Pin id. | Pin name       | Description                                         | Voltage |
|---------|----------------|-----------------------------------------------------|---------|
| 1       | GND            | Ground                                              |         |
| 2       | +3.3V          | 3.3 V power supply                                  |         |
| 3       | USB_D+         | USB high-, full-, and low- speed data pair positive |         |
| 4       | +3.3V          | 3.3 V power supply                                  |         |
| 5       | USB_D-         | USB high-, full-, and low- speed data pair negative |         |
| 6       | LED1#          | M2_WL_LED-                                          |         |
| 7       | GND            | Ground                                              |         |
| 8       | N/A            |                                                     |         |
| 9       | N/A            |                                                     |         |
| 10      | N/A            |                                                     |         |
| 11      | N/A            |                                                     |         |
| 12      | N/A            |                                                     |         |
| 13      | N/A            |                                                     |         |
| 14      | N/A            |                                                     |         |
| 15      | N/A            |                                                     |         |
| 16      | LED2#          | M2_BT_LED-                                          |         |
| 17      | N/A            |                                                     |         |
| 18      | GND            | Ground                                              |         |
| 19      | N/A            |                                                     |         |
| 20      | WAKE#          | M2_BT_WAKE-                                         | 0/3.3V  |
| 21      | N/A            |                                                     |         |
| 22      | N/A            |                                                     |         |
| 23      | N/A            |                                                     |         |
| 24-31   | Key E          | Substrate removed to act as physical key            |         |
| 32      | N/A            |                                                     |         |
| 33      | GND            | Ground                                              |         |
| 34      | N/A            |                                                     |         |
| 35      | PETp0          | PCI Express lane 0 module transmitter pair positive |         |
| 36      | N/A            |                                                     |         |
| 37      | PETn0          | PCI Express lane 0 module transmitter pair negative |         |
| 38      | Devic WAKE#    | BT_DEV_WAKE-                                        | 0/3.3V  |
| 39      | GND            | Ground                                              |         |
| 40      | N/A            |                                                     |         |
| 41      | PERp0          | PCI Express lane 0 module receiver pair positive    |         |
| 42      | N/A            |                                                     |         |
| 43      | PERn0          | PCI Express lane 0 module receiver pair negative    |         |
| 44      | N/A            |                                                     |         |
| 45      | GND            | Ground                                              |         |
| 46      | N/A            |                                                     |         |
| 47      | PEFCLKP0       | PCI Express reference clock pair positive           |         |
| 48      | N/A            |                                                     |         |
| 49      | PEFCLKN0       | PCI Express reference clock pair negative           |         |
| 50      | SUSCLK         | 32.768 kHz clock module input                       | 0/3.3V  |
| 51      | GND            | Ground                                              |         |
| 52      | PERSTO#        | PCI Express reset                                   | 0/3.3V  |
| 53      | CLKREQ0#       | PCI Express clock request                           | 0/3.3V  |
| 54      | W_DISABLE2#    | Wireless disable 2                                  | 0/3.3V  |
| 55      | PEWake0#       | PCI Express wake                                    | 0/3.3V  |
| 56      | W_DISABLE1#    | Wireless disable 1                                  | 0/3.3V  |
| 57      | GND            | Ground                                              |         |
| 58      | N/A            |                                                     |         |
| 59      | N/A            |                                                     |         |
| 60      | N/A            |                                                     |         |
| 61      | N/A            |                                                     |         |
| 62      | N/A            |                                                     |         |
| 63      | GND            | Ground                                              |         |
| 64      | N/A            |                                                     |         |
| 65      | N/A            |                                                     |         |
| 66      | N/A            |                                                     |         |
| 67      | Reserved/PERn1 |                                                     |         |
| 68      | N/A            |                                                     |         |
| 69      | GND            | Ground                                              |         |
| 70      | N/A            |                                                     |         |
| 71      | N/A            |                                                     |         |
| 72      | +3.3V          | power supply                                        | 3.3 V   |
| 73      | N/A            |                                                     |         |
| 74      | +3.3V          | power supply                                        | 3.3 V   |
| 75      | GND            | Ground                                              |         |

## M.2 M-key 2280– Supports PCIe x4 NVMe & SATA SSD Storage

| Pin id. | Pin name        | Description                                                               | Voltage |
|---------|-----------------|---------------------------------------------------------------------------|---------|
| 1       | NC              | No Connect                                                                |         |
| 2       | 3.3 V           | Supply pin                                                                | 3.3 V   |
| 3       | GND             | Ground                                                                    |         |
| 4       | 3.3 V           | Supply pin                                                                | 3.3 V   |
| 5       | PERn3           | PCIe Lane 3 Rx                                                            |         |
| 6       | N/A             |                                                                           |         |
| 7       | PERp3           | PCIe Lane 3 Rx                                                            |         |
| 8       | N/A             |                                                                           |         |
| 9       | GND             | Ground                                                                    |         |
| 10      | DAS/DSS         | Device Activity Signal / Disable Staggered Spinup                         |         |
| 11      | PETn3           | PCIe Lane 3 Tx                                                            |         |
| 12      | 3.3 V           | Supply pin                                                                | 3.3 V   |
| 13      | PETp3           | PCIe Lane 3 Tx                                                            |         |
| 14      | 3.3 V           | Supply pin                                                                | 3.3 V   |
| 15      | GND             | Ground                                                                    |         |
| 16      | 3.3V            | Supply pin                                                                | 3.3 V   |
| 17      | PERn2           | PCIe Lane 2 Rx                                                            |         |
| 18      | 3.3 V           | Supply pin                                                                | 3.3 V   |
| 19      | PERp2           | PCIe Lane 2 Rx                                                            |         |
| 20      | N/A             |                                                                           |         |
| 21      | GND             | Ground                                                                    |         |
| 22      | N/A             |                                                                           |         |
| 23      | PETn2           | PCIe Lane 2 Tx                                                            |         |
| 24      | N/A             |                                                                           |         |
| 25      | PETp2           | PCIe Lane 2 Tx                                                            |         |
| 26      | N/A             |                                                                           |         |
| 27      | GND             | Ground                                                                    |         |
| 28      | N/A             |                                                                           |         |
| 29      | PERn1           | PCIe Lane 1 Rx                                                            |         |
| 30      | N/A             |                                                                           |         |
| 31      | PERp1           | PCIe Lane 1 Rx                                                            |         |
| 32      | N/A             |                                                                           |         |
| 33      | GND             | Ground                                                                    |         |
| 34      | N/A             |                                                                           |         |
| 35      | PETn1           | PCIe Lane 1 Tx                                                            |         |
| 36      | N/A             |                                                                           |         |
| 37      | PETp1           | PCIe Lane 1 Tx                                                            |         |
| 38      | N/A             |                                                                           |         |
| 39      | GND             | Ground                                                                    |         |
| 40      | N/A             |                                                                           |         |
| 41      | SATA-B+/PERn0   | Host receiver differential signal pair. If in PCIe mode PCIe Lane 0 Rx    |         |
| 42      | N/A             |                                                                           |         |
| 43      | SATA-B-/PERp0   | Host receiver differential signal pair. If in PCIe mode PCIe Lane 0 Rx    |         |
| 44      | N/A             |                                                                           |         |
| 45      | GND             | Ground                                                                    |         |
| 46      | N/A             |                                                                           |         |
| 47      | SATA-A-/PETn0   | Host transmitter differential signal pair. If in PCIe mode PCIe Lane 0 Tx |         |
| 48      | N/A             |                                                                           |         |
| 49      | SATA-A+/PETp0   | Host transmitter differential signal pair. If in PCIe mode PCIe Lane 0 Tx |         |
| 50      | PERST#          | PCIe reset                                                                |         |
| 51      | GND             | Ground                                                                    |         |
| 52      | CLKREQ#         | Reference clock request signal                                            |         |
| 53      | REFCLKN         | PCIe Reference Clock signals (100 MHz)                                    |         |
| 54      | PEWAKE#         | PCIe WAKE# Open Drain with pull up on platform. Active Low.               |         |
| 55      | REFCLKP         | PCIe Reference Clock signals (100 MHz)                                    |         |
| 56      | N/A             |                                                                           |         |
| 57      | GND             | Ground                                                                    |         |
| 58      | N/A             |                                                                           |         |
| 59-66   | removed (Key M) | Mechanical notch M                                                        |         |
| 67      | N/A             |                                                                           |         |
| 68      | SUSCLK          | 32.768 kHz clock supply input provided by the Platform chipset            |         |
| 69      | CONFIG_1        | Defines module type (0 :SATA 1:NVME)                                      |         |
| 70      | 3.3 V           | Supply pin                                                                | 3.3 V   |
| 71      | GND             | Ground                                                                    |         |
| 72      | 3.3 V           | Supply pin                                                                | 3.3 V   |
| 73      | GND             | Ground                                                                    |         |
| 74      | 3.3 V           | Supply pin                                                                | 3.3 V   |
| 75      | GND             | Ground                                                                    |         |

# 2-3 Connecting Cables and Jumper Settings

This section takes you through all the necessary connections on the mainboard.

## Front Panel Header

The front panel header (CFP1, 2.54mm pitch) on this motherboard is used to connect the front panel switches and LEDs.

► **PWR\_LED**

Attach the front panel power LED cable to these two pins of the connector. The Power LED indicates the system's status.

| System Status | Power LED indicates |
|---------------|---------------------|
| S0            | The LED is on       |
| S5            | The LED is off      |
| S3            | The LED will blink  |
| S4            | The LED is off      |

► **PW\_ON**

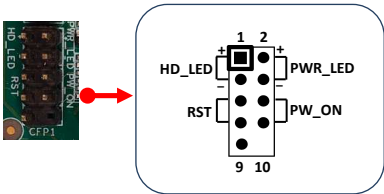
Attach the power button cable from the case to these two pins. Pressing the power button on the front panel turns the system on and off rather than using the onboard button.

► **HD\_LED**

Attach the hard disk drive indicator LED cable to these two pins. The HDD indicator LED indicates the activity status of the hard disks.

► **RESET**

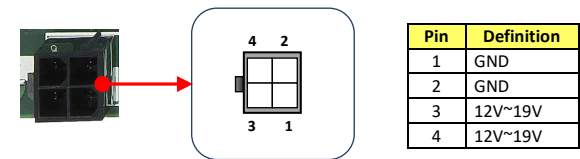
Attach the Reset switch cable from the front panel of the case to these two pins. The system restarts when the RESET switch is pressed.



| Header     | Pin | Signal    |
|------------|-----|-----------|
| HD_LED     | 1   | HD_PWR    |
|            | 3   | HD Active |
| PWRLED     | 2   | PWR LED+  |
|            | 4   | PWR LED-  |
| RESET      | 5   | Ground    |
|            | 7   | RST BTN   |
| PWRSW      | 6   | PWR BTN   |
|            | 8   | Ground    |
| No Connect | 9   | +5V       |
| Empty      | 10  | Empty     |

### 4-pin 12V~19V Power Connector

PW1, This power connector is used to provide power to the system. Align the power plug to the connector and press firmly until seated.



DC-in Jack (CN3)

**Note 1:**  
There are two ways to source power to the board: DC-in jack or 4-pin power connector. Two different physical ports that can only be used one at a time.  
e.g. When DC-in 12V ~ 19V jack is being used, the 4-pin power connector shouldn't be connected to any power source.

**Warning:**  
One of the power inputs may be damaged when connecting both DC jack and 4-pin power connector at the same time.

### PW1 Power Usage:

PW1 can serve as the power input for the VPR platform, as an alternative to the rear panel DC jack (CN3).

Please note that only one power input — either PW1 or CN3 — should be used at a time. Do not connect power to both simultaneously.

When using an expansion daughtercard that requires a 12V power supply (such as the GMSL daughtercard) and planning to distribute power internally through PW1, please follow the configuration below:

- Use CN3 (DC jack) as the sole power input.
- Use an external power supply that outputs 12V.
  - Although the mainboard supports an input voltage range of approximately 12V to 19V, the daughtercard requires a fixed 12V input voltage.

### Caution:

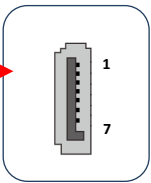
When using the GMSL daughtercard, do not apply an input voltage higher than 12V to avoid damage to the daughtercard.

If supplying power through PW1, please ensure that the voltage requirements of any other connected daughtercards are compatible with the main power input.

---

### SATA3 Connector

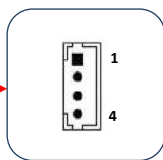
The S1 is SATA3 Connectors and works at speeds of up to 6G/s. Each cable can be used to connect one SATA drive to the mainboard.



| Pin | Definition |
|-----|------------|
| 1   | GND        |
| 2   | TX+        |
| 3   | TX-        |
| 4   | GND        |
| 5   | RX-        |
| 6   | RX+        |
| 7   | GND        |

### SATA Power Header

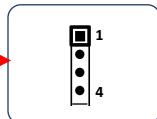
The SATA Power header is used to provide 5V and 12V power to SATA3 connector.



| Pin | Definition |
|-----|------------|
| 1   | +12V       |
| 2   | GND        |
| 3   | GND        |
| 4   | +5V        |

### USB2.0 Header

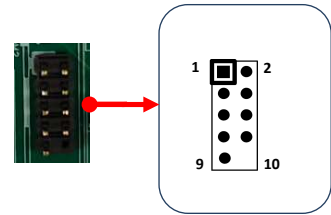
This mainboard contains one 4-pin onboard header (USB2-A, 2.54mm pitch) that can be used to connect to one (1) external USB 2.0 device.



| Pin | Definition |
|-----|------------|
| 1   | VCC        |
| 2   | USB0-      |
| 3   | USB0+      |
| 4   | GND        |

### COM Header

The Serial port header (COM2, 2.54mm pitch) can provide one serial port via an optional COM port cable.

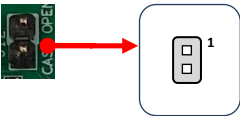


| Pin | Definition | Pin | Definition |
|-----|------------|-----|------------|
| 1   | DCD        | 2   | RXD        |
| 3   | TXD        | 4   | DTR        |
| 5   | GND        | 6   | DSR        |
| 7   | RTS        | 8   | CTS        |
| 9   | RI#        | 10  | Empty      |

Note:  
The pin definition of header and standard DB9 male pin out is different.

### Case Open Header

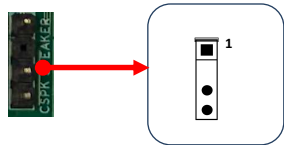
This header (J12, 2.54mm pitch) is used to for a chassis open detect. When set, the warning message will appear during POST when the case is opened.



| Pin | Definition |
|-----|------------|
| 1   | Case Open  |
| 2   | GND        |

### Speaker Header

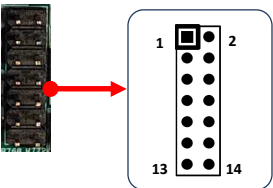
This header (CSPK, 2.54mm pitch) is used to connect the case's speaker for PC beeps.



| Pin | Definition  |
|-----|-------------|
| 1   | Speaker out |
| 2   | Empty       |
| 3   | GND         |
| 4   | GND         |

### AMD FPGA JTAG Port (Internal Use Only)

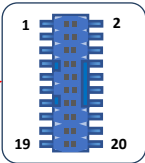
This header (J2, 2.54mm pitch)



| Pin | Definition | Pin | Definition |
|-----|------------|-----|------------|
| 1   | GND        | 2   | +1.8V      |
| 3   | GND        | 4   | VE2302_TMS |
| 5   | GND        | 6   | VE2302_TCK |
| 7   | GND        | 8   | VE2302_TDO |
| 9   | GND        | 10  | VE2302_TDI |
| 11  | GND        | 12  | NC         |
| 13  | GND        | 14  | RESET-     |

### AMD APU HDT+ Header (Internal Use Only)

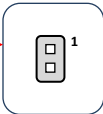
This header (J5, 1.27mm pitch)



| Pin | Definition | Pin | Definition |
|-----|------------|-----|------------|
| 1   | +1.8V_ALW  | 2   | APU_TCK    |
| 3   | GND        | 4   | APU_TMS    |
| 5   | GND        | 6   | APU_TDI    |
| 7   | GND        | 8   | APU_TDO    |
| 9   | APU_TRST-  | 10  | APU_PWRGD  |
| 11  | GND        | 12  | RESET-     |
| 13  | GND        | 14  | NC         |
| 15  | GND        | 16  | APU_DBREQ- |
| 17  | GND        | 18  | NC         |
| 19  | +1.8V_ALW  | 20  | NC         |

### VE2302 GPIO1 Header

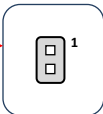
This header (J6, 2.54mm pitch)



| Pin | Definition  |
|-----|-------------|
| 1   | FuSa_GPIO_1 |
| 2   | GND         |

### AMD APU HDT Warm Reset Header (Internal Use Only)

This header (J7, 2.54mm pitch)



| Pin | Definition |
|-----|------------|
| 1   | APU Reset- |
| 2   | GND        |

### VE2302 GPIO2 Header

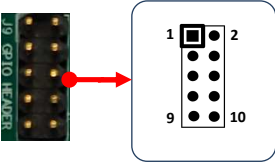
This header (J8, 2.54mm pitch)



| Pin | Definition  |
|-----|-------------|
| 1   | FuSa_GPIO_2 |
| 2   | GND         |

## AMD GPIO Header

There is a GPIO (General-purpose input/output) header (J9, 2.54mm pitch) on the motherboard. It can connect a variety of simple one- or two-wire devices.



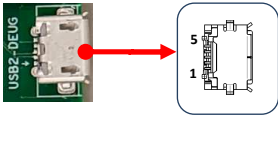
| Pin | Definition | Pin | Definition |
|-----|------------|-----|------------|
| 1   | GPIO       | 2   | GPIO       |
| 3   | GPIO       | 4   | GPIO       |
| 5   | GPIO       | 6   | GPIO       |
| 7   | GPIO       | 8   | GPIO       |
| 9   | +3.3V_ALW  | 10  | GND        |

## External USB INPUT Connector (USB2-DEUG) (Select by JP4)

When the JP4 plug connects pins 1-2, the FPGA debug USB port source is from internal USB 2.0 port of APU.

When the JP4 plug connects pins 2-3, the FPGA debug USB port source is from an external computer through the micro-USB port (USB2-DEUG connector).

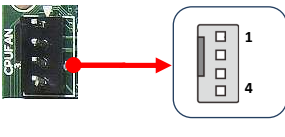
The user needs to supply a standard USB micro USB to Type A cable for this connection.



| Pin | Definition |
|-----|------------|
| 1   | NC         |
| 2   | USB2_D-    |
| 3   | USB2_D+    |
| 4   | NC         |
| 5   | GND        |

## Fan Headers

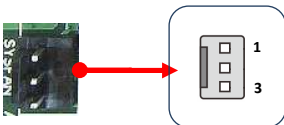
There are two headers (CPUFAN and SYSFAN, 2.54mm pitch) on the motherboard. These fans can be speed detected/controlled and displayed in the Hardware Health Configuration section of the CMOS Setup. The fans are automatically turned off after the system enters S3, S4 or S5 mode.



| Pin | Definition |
|-----|------------|
| 1   | GND        |
| 2   | +12V       |
| 3   | Sense      |
| 4   | Control    |

Note:

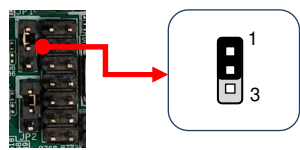
The CPU fan cable can be either a 3-pin or a 4-pin connector. Connect a 3-pin connector to pins 1, 2, and 3 on the mainboard connector.



| Pin | Definition |
|-----|------------|
| 1   | GND        |
| 2   | +12V       |
| 3   | Sense      |

### PSLP Power Control Jumper (JP1)

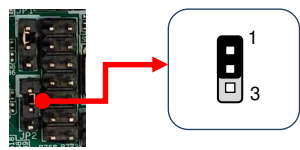
You can use JP1 (2.54mm pitch) to select to enable or disable the PSLP Power function.



| Pin | Settings                        |
|-----|---------------------------------|
| 1-2 | Enable VCC_PSLP Power (Default) |
| 2-3 | Disable VCC_PSLP Power          |

### PSFP Power Control Jumper (JP2)

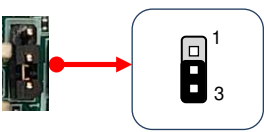
You can use JP2 (2.54mm pitch) to select to enable or disable the PSFP Power function.



| Pin | Settings                        |
|-----|---------------------------------|
| 1-2 | Enable VCC_PSFP Power (Default) |
| 2-3 | Disable VCC_PSFP Power          |

### FUSE Power Control Jumper (JP3)

You can use JP3 (2.54mm pitch) to select to enable or disable the FUSE Power Control function.



| Pin | Settings                        |
|-----|---------------------------------|
| 1-2 | Enable Burn the FUSE            |
| 2-3 | Disable Burn the FUSE (Default) |

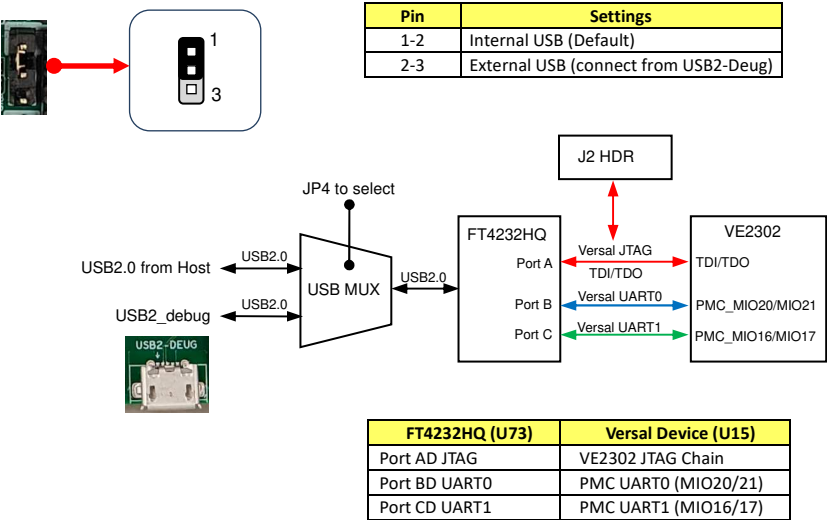
### USB Debug Port Selection Jumper of VE2302 (JP4)

The Versal AI Edge VE2302 FPGA is connected to a USB 2.0 interface via an FTDI FT4232 USB-to-JTAG/USB-UART device, providing access for debugging purposes.

There are two debug USB port that are selected by JP4.

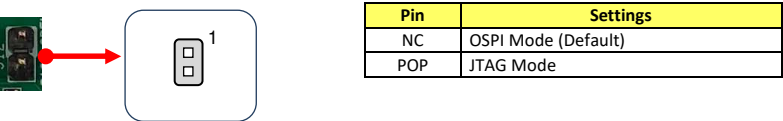
When the JP4 plug connects pins 1-2, the FPGA debug USB port source is from internal USB 2.0 port of APU.

When the JP4 plug connects pins 2-3, the FPGA debug USB port source is from an external computer through the micro-USB port (USB2-DEUG connector).



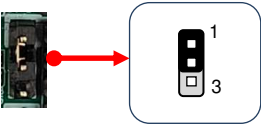
### VE2302 MODE Selection Jumper (JP5)

You can use JP5 (2.54mm pitch) for VE2302 MODE selection.



### ROM Write Protect mode Jumper (JP6)

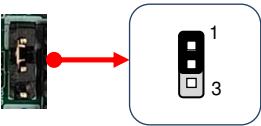
You can use JP6 (2.54mm pitch) for ROM Write Protect mode selection.



| Pin | Settings                |
|-----|-------------------------|
| 1-2 | Write Protect (Default) |
| 2-3 | Write Operations        |

### Versal Power Control Jumper (JP7)

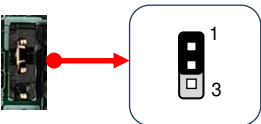
You can use JP7 (2.54mm pitch) for Versal Power Control.



| Pin | Settings                             |
|-----|--------------------------------------|
| 1-2 | Enable All of Versal Power (Default) |
| 2-3 | Disable All of Versal Power          |

### Main Power Control Jumper (JP8)

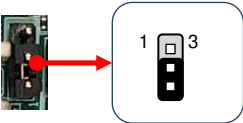
You can use JP8 (2.54mm pitch) for Main Power Control.



| Pin | Settings                    |
|-----|-----------------------------|
| 1-2 | Enable Main Power (Default) |
| 2-3 | Disable Main Power          |

### Auto Power ON Jumper (JP9)

You can use JP9 (2.54mm pitch) to select to enable or disable the auto power on function.

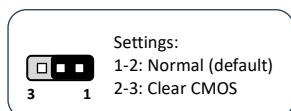


| Pin | Settings                                                                                           |
|-----|----------------------------------------------------------------------------------------------------|
| 1-2 | Disable.<br>Press power button manually to power on after power input is connected to power source |
| 2-3 | Enable.<br>Automatically power on when power input is connected to power source (Default)          |

---

## Clear CMOS Jumper (CMOS1)

This mainboard contains a jumper (CMOS1) that can clear CMOS data. If the CMOS data becomes corrupted or you forgot the supervisor or user password, clear the CMOS data to reconfigure the system back to the default values stored in the ROM BIOS.



---

To clear CMOS data, please follow the steps below.

1. Turn off the system.
  2. Change the jumper from “1-2” to “2-3” position for a few seconds.
  3. Replace the jumper back to the “1-2” position.
  4. Turn on the system and hold down the <Del> key to enter BIOS Setup.
-

---

## 2-4 System LED Status Indicators

This mainboard provides three LEDs to indicate the system's status.

- STANDBY LED (LED10, Blue): When the System is in Standby Mode, this LED is on. This LED will remain on as long as the motherboard is receiving constant power.
- POWER LED (LED11, Green): When the System is powered on, this LED is on.
- DIMM LED (LED12, Yellow): When the Memory slot is functional, this LED is on.
- Versal DONE LED (LED6, Green): Indicates the AMD VE2302's done status.
- Versal ERROR LED (LED7, Red): Indicates the AMD VE2302's error status.



## 2-5 Minimum connection required to boot

A motherboard in its minimal boot configuration requires only the following:

- RAM: 8GB, 2 x 4GB DDR4
- Storage: a 512GB SSD
- Power Supply: 120W (Recommended)
- Monitor: HDMI or DP Monitor
- Keyboard and Mouse: USB Keyboard and Mouse

---

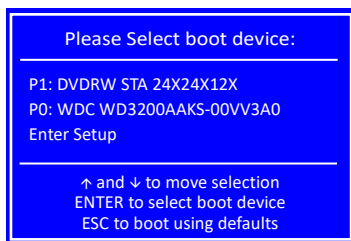
## **Chapter 3 Configuring the BIOS**

This chapter provides information on the BIOS Setup program and allows you to configure the system for optimum use.

### ***3-1 Select Boot Device***

Select Boot Device Menu allows you to set the first boot device without entering BIOS Setup.

During Power On Self Test (POST), you can press the <**F7**> key to enter select boot device menu. The system will directly boot from the device configured in Boot Menu.



### ***3-2 Enter BIOS Setup***

The BIOS is the communication bridge between hardware and software. Correctly setting the BIOS parameters is critical to maintain optimal system performance.

Use the following procedure to change BIOS settings.

1. Power on the computer.
2. Press the <**Del**> or <**F2**> key to enter BIOS Setup during BIOS Power On Self Test (POST).

📌 Note1: You do not "need" to update the BIOS when receiving your system - it is shipped with working BIOS setting.

📌 Note2: It is strongly recommended that you do not change the default BIOS settings. Changing some settings could damage your computer.

---

 Note3: The BIOS options in this manual are for reference only. BIOS screens in manuals are usually the first BIOS version when the board is released and may be different from your purchased motherboard. Users are welcome to download the latest BIOS version from our official website.

## Control Keys

Please check the following table for the function description of each Control key.

| Control Key(s) | Function Description                                  |
|----------------|-------------------------------------------------------|
| → / ←          | Moves cursor left or right to select screens          |
| ↑ / ↓          | Moves cursor up or down to select items               |
| <Enter>        | To bring up the selected item                         |
| + / -          | To change option for the selected items               |
| <F1>           | To display the General Help Screen                    |
| <F2>           | To load previous values for all the settings          |
| <F3>           | To load optimized default values for all the settings |
| <F4>           | To save changes and exit the setup utility            |
| <ESC>          | To jump to the Exit Screen or exit the current screen |

### 3-3 Main Menu

When entering the Aptio Setup Utility, the main menu screen appears. This main menu includes the system overview and displays the basic system configuration, such as BIOS information, memory size and system date/time.

| Aptio Setup - AMI                        |          |                         |          |                                                                                                                                                                                |             |
|------------------------------------------|----------|-------------------------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| Main                                     | Advanced | Chipset                 | Security | Boot                                                                                                                                                                           | Save & Exit |
| BIOS Information                         |          |                         |          | Set the Date. Use Tab to switch between Date elements.<br>Default Ranges:<br>Year: 1998-9999<br>Months: 1-12<br>Days: Dependent on month<br>Range of Year may vary.            |             |
| BIOS Vendor                              |          | American Megatrends     |          |                                                                                                                                                                                |             |
| Core Version                             |          | 5.24                    |          |                                                                                                                                                                                |             |
| Compliance                               |          | UEFI 2.8; PI 1.7        |          |                                                                                                                                                                                |             |
| Project Version                          |          | V020 (I907W020.ROM) x64 |          |                                                                                                                                                                                |             |
| Build Date and Time                      |          | 12/01/2023 14:24:53     |          | →←: Select Screen<br>↑↓: Select Item<br>Enter: Select<br>+/-: Change Opt.<br>F1: General Help<br>F2: Previous Values<br>F3: Optimized Defaults<br>F4: Save & Exit<br>ESC: Exit |             |
| Access Level                             |          | Administrator           |          |                                                                                                                                                                                |             |
| Memory Information                       |          |                         |          |                                                                                                                                                                                |             |
| Total Memory                             |          | 32768 MB (DDR4-2667)    |          |                                                                                                                                                                                |             |
| System Date                              |          | [Tue 01/23/2024]        |          |                                                                                                                                                                                |             |
| System Time                              |          | [10:45:26]              |          |                                                                                                                                                                                |             |
| Version 2.22.1282 Copyright (C) 2023 AMI |          |                         |          |                                                                                                                                                                                |             |

#### BIOS Information

This field displays the current BIOS version, build date and ID information etc..

#### Memory Information

Displays current system memory size.

#### System Date

Allows you to set the system date. The format is <Day> <Month> <Date> <Year>.

[Day] Weekday from Sun. to Sat., this is automatically displayed by BIOS.

[Month] The month from 1 to 12.

[Date] The date from 1 to 31 can be keyed by numeric function keys.

[Year] The year can be adjusted by users.

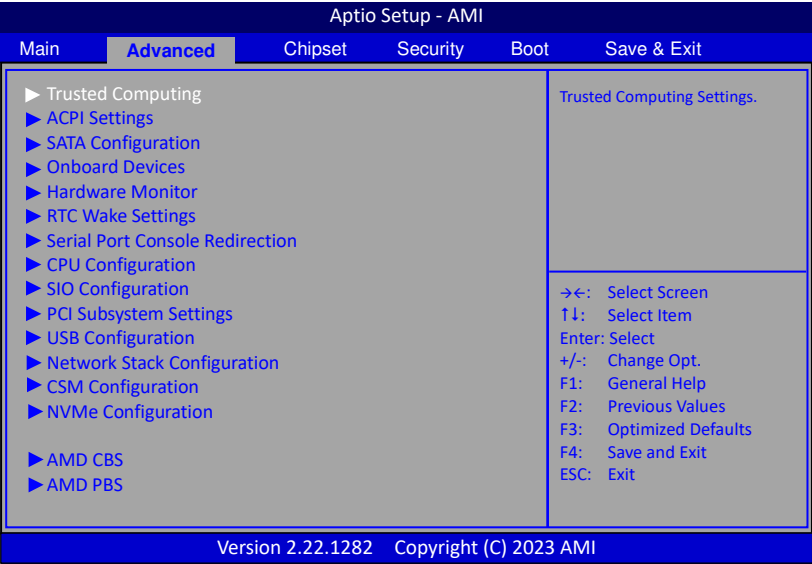
#### System Time

Allows you to set the system time. The time format is

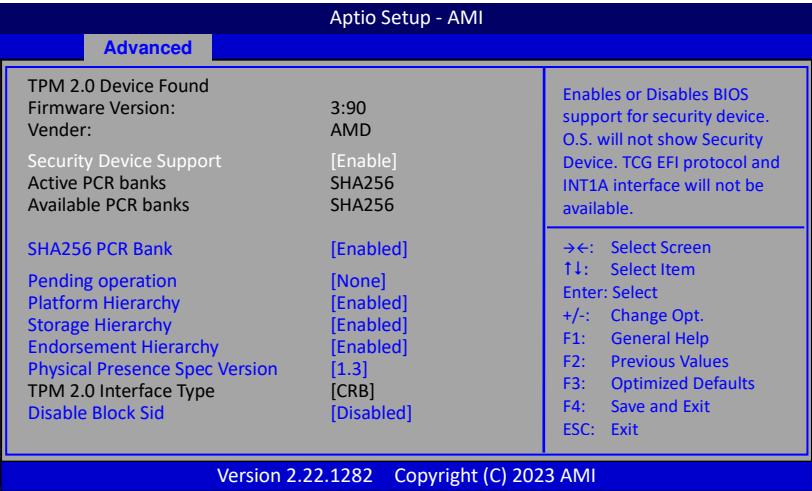
<hour>:<minute>:<second>.

### 3-4 Advanced Menu

The Advanced menu items allow you to change the settings for the CPU, USB and other system devices. Press <Enter> to display the configuration options.



► **Trusted Computing**



---

### **Security Device Support**

Enables or disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available. When enabled, the related items will appear.

Options: Enabled, Disabled.

### **SHA256 PCR Bank**

Enable or disable SHA256 PCR Bank.

Options: Enabled, Disabled.

### **Pending operation**

Schedule an Operation for the Security Device.

NOTE: Your Computer will reboot during restart in order to change State of Security Device.

Options: None, TPM Clear.

### **Platform Hierarchy**

Enables or disable Platform Hierarchy.

Options: Enabled, Disabled.

### **Storage Hierarchy**

Enables or disable Storage Hierarchy.

Options: Enabled, Disabled.

### **Endorsement Hierarchy**

Enables or disable Endorsement Hierarchy.

Options: Enabled, Disabled.

### **Physical Presence Spec Version**

Select to Tell O.S. to support PPI Spec version 1.2 or 1.3. Note some HCK tests might not support 1.3.

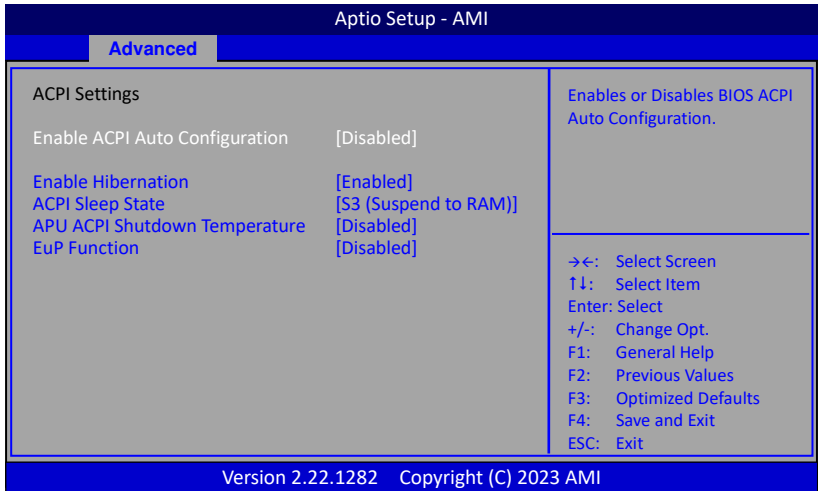
Options: 1.2, 1.3.

### **Disable Block Sid**

Override to allow SID authentication in TCG Storage device.

Options: Enabled, Disabled.

► **ACPI Settings**



**Enable ACPI Auto Configuration**

This item allows you to enable or disable BIOS ACPI Auto Configuration.  
Options: Enabled, Disabled.

**Enable Hibernation**

This item allows you to enable system ability to Hibernate (OS/S4 Sleep Sate).  
This option may be not effective with some OS.  
Options: Enabled, Disabled.

**ACPI Sleep State**

Allow you to select the power saving modes for ACPI function.  
Options: Suspend Disabled, S3 (Suspend to RAM).

**APU ACPI Shutdown Temperature**

If the APU temperature is higher than ACPI shutdown temperature, the system will shut down. When set to "Enabled" option. The following items will appear.

**Shutdown Temperature**

Allows you set a value of temperature for system shutdown.  
The default is 80.

**EuP Function**

Enables the EuP (Energy Using Products) function, allows BIOS to switch off some power at S5 state to get system ready for the EuP requirement to reduce power consumption.  
Options: Enabled, Disabled.

► **SATA Configuration**

Aptio Setup - AMI

Advanced

SATA Configuration

SATA Port 0 (M.2 M-Key)SAMSUNG SSD 885 (256.0GB)

SATA Port 1Not Present

→←: Select Screen

↑↓: Select Item

Enter: Select

+/-: Change Opt.

F1: General Help

F2: Previous Values

F3: Optimized Defaults

F4: Save and Exit

ESC: Exit

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**SATA Port 0 (M.2 M-Key) / SATA Port 1**

This field shows SATA ports connection state.

► **Onboard Devices**

Aptio Setup - AMI

Advanced

► PCI-E Port

► Case Open Configuration

HD Audio Azalia Device[Enabled]

WatchDog Timer[Disabled]

► GPIO Header Control

COM1 Mode Selection[RS232]

COM2 Mode Selection[RS232]

PCI-E Port Parameters

→←: Select Screen

↑↓: Select Item

Enter: Select

+/-: Change Opt.

F1: General Help

F2: Previous Values

F3: Optimized Defaults

F4: Save and Exit

ESC: Exit

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---

## **PCI-E Port**

### **XILINX Versal VE2302 (PCIE 4)**

Allows you to enable or disable the onboard XILINX Versal VE2302.

Options: Enabled, Disabled.

#### **ASM Mode Control**

NB Root Port ASPM Mode Control.

Options: Disabled, L0S Entry, L1 Entry, L0S and L1 Entry, Auto.

#### **Hotplug Mode Control**

NB Root Hotplug Mode Control.

Options: Disabled, Hotplug Basic, Hotplug Server, Hotplug Enhanced, Hotplug Inboard, Auto.

#### **Fixed I/O Resources**

Fixed PCI I/O Resources.

Options: Disabled, 4K, 8K, 16K, 32K.

#### **Fixed MMIO 32 bit Resources**

Fixed PCI MMIO 32 bit Resources.

Options: Disabled, 1M, 2M, 4M, 8M, 16M, 32M, 64M, 128M.

#### **Fixed PFMMIO 32 bit Resources**

Fixed PCI MMIO 32 bit Prefetchable Resources.

Options: Disabled, 1M, 2M, 4M, 8M, 16M, 32M, 64M, 128M.

#### **Fixed PFMMIO 64 bit Resources**

Fixed PCI MMIO 32 bit Prefetchable Resources.

Options: Disabled, 1M, 2M, 4M, 8M, 16M, 32M, 64M, 128M, 256M, 512M, 1G, 2G, 4G, 8G.

## **M.2 M-Key Socket (PCIE x4)**

Allows you to enable or disable the M.2 M-Key Socket.

Options: Disabled, Enabled.

#### **ASM Mode Control**

NB Root Port ASPM Mode Control.

Options: Disabled, L0S Entry, L1 Entry, L0S and L1 Entry, Auto.

#### **Hotplug Mode Control**

NB Root Hotplug Mode Control.

Options: Disabled, Hotplug Basic, Hotplug Server, Hotplug Enhanced, Hotplug Inboard, Auto.

## **M.2 E-Key Socket (PCIE x1)**

Allows you to enable or disable the M.2 E-Key Socket.

Options: Disabled, Enabled.

---

### **ASM Mode Control**

NB Root Port ASPM Mode Control.

Options: Disabled, L0S Entry, L1 Entry, L0S and L1 Entry, Auto.

### **Hotplug Mode Control**

NB Root Hotplug Mode Control.

Options: Disabled, Hotplug Basic, Hotplug Server, Hotplug Enhanced, Hotplug Inboard, Auto.

### **Onboard 2.5 Gigabit LAN (PCIE x1)**

Allows you to enable or disable the onboard LAN controller.

Options: Enabled, Disabled.

### **ASM Mode Control**

NB Root Port ASPM Mode Control.

Options: Disabled, L0S Entry, L1 Entry, L0S and L1 Entry, Auto.

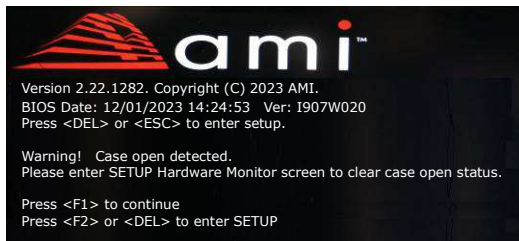
### **Hotplug Mode Control**

NB Root Hotplug Mode Control.

Options: Disabled, Hotplug Basic, Hotplug Server, Hotplug Enhanced, Hotplug Inboard, Auto.

### **Case Open Configuration**

The chassis intrusion detection alerts you whenever your computer chassis was opened. If the case cover is opened, the system will automatically restart and appear prompt message (Shown below) during POST.



### **HD Audio Azalia Device**

Allows you to enable or disable the onboard High Definition Audio controller.

Options: Disabled, Enabled.

### **WatchDog Timer**

Allow you to enable WatchDog timer expires during OS boot. When set to "Enabled" option. The following items will appear.

---

### Time of watchdog timer (second)

Allows you set a period of seconds for watchdog timer.

Options: 5 ~ 255 second.

### GPIO Header Control

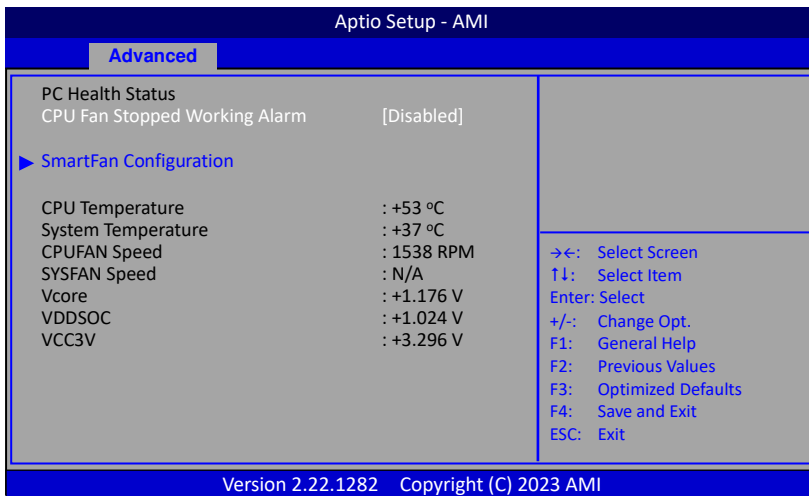
This sub-item is for GPIO (General-purpose input/output) header control, each GPIO is accessible via a connector pin.

### COM1 Mode Selection / COM2 Mode Selection

Allows you to select RS232/RS485/RS422 Mode.

Options: RS422, RS232, RS485 Receiver Half Duplex, RS485 Driver Half Duplex.

## ► Hardware Monitor



### CPU Fan Stopped Working Alarm

When the cooler is damaged or the APU fan connector is not connected even other factors affecting fan operation, the APU Fan will be stopped working. Meanwhile the system will automatically restart and appear prompt message (Shown below) during POST.

You can make a selection to enter the system.



## ► Smart Fan Configuration

| Aptio Setup - AMI                        |            |                        |
|------------------------------------------|------------|------------------------|
| Advanced                                 |            |                        |
| SmartFan Configuration                   |            | Fan Mode Setting       |
| CPUFan Mode Setting                      | [SmartFan] |                        |
| Highest Fan Speed In Percentage          | 100        |                        |
| 1st Temperature Threshold (°C)           | 80         |                        |
| 2nd Fan Speed In Percentage              | 70         |                        |
| 2nd Temperature Threshold (°C)           | 70         |                        |
| 3rd Fan Speed In Percentage              | 50         | →←: Select Screen      |
| 3rd Temperature Threshold (°C)           | 55         | T↓: Select Item        |
| 4th Fan Speed In Percentage              | 30         | Enter: Select          |
| 4th Temperature Threshold (°C)           | 40         | +/-: Change Opt.       |
| Lowest Fan Speed In Percentage           | 10         | F1: General Help       |
|                                          |            | F2: Previous Values    |
|                                          |            | F3: Optimized Defaults |
|                                          |            | F4: Save and Exit      |
|                                          |            | ESC: Exit              |
| System Fan Mode Setting                  | [SmartFan] |                        |
| Highest Fan Speed In Percentage          | 100        |                        |
| 1st Temperature Threshold (°C)           | 80         |                        |
| 2nd Fan Speed In Percentage              | 70         |                        |
| 2nd Temperature Threshold (°C)           | 70         |                        |
| 3rd Fan Speed In Percentage              | 50         |                        |
| 3rd Temperature Threshold (°C)           | 55         |                        |
| 4th Fan Speed In Percentage              | 30         |                        |
| 4th Temperature Threshold (°C)           | 40         |                        |
| Lowest Fan Speed In Percentage           | 10         |                        |
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### APUFan Mode Setting / System Fan Mode Setting

This item controls the speed of the various fans on the motherboard.

SmartFan: When you want the speed of the fans automatically controlled based on temperature.

Manual By DutyCycle: To set the fan speed to a constant rate, the speed from 0% to 100%.

Manual By RPM: This item sets the fan speed at a fixed.

### APU / System Temperature

Displays the current APU / System Temperature.

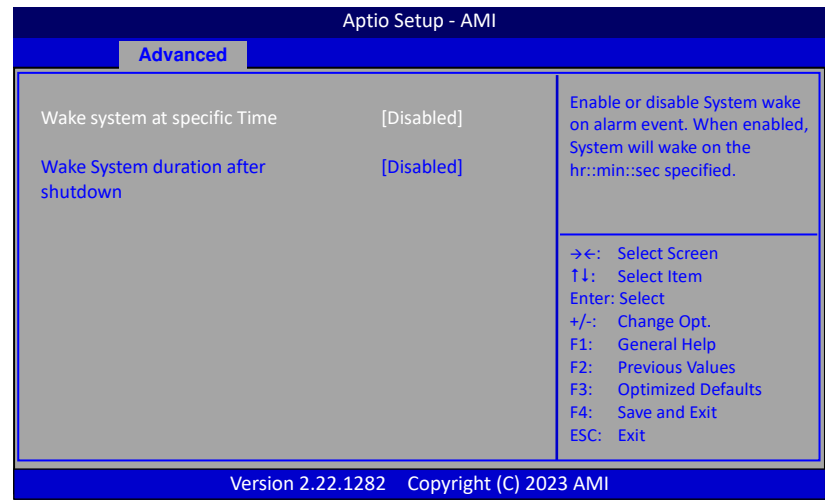
**CPUFAN Speed / SYSFAN Speed**

Displays the current APU / System Fan Speeds.

**Vcore / VDDSOC / VCC3V**

The current voltages are automatically detected and displayed by the system.

► **RTC Wake Settings**



**Wake system at specific Time**

Enable or disable system wakeup on alarm event. When enabled, the related items will appear.

Options: Enabled, Disabled.

**Wake up days of the week**

This item allows you to select days of the week to wake up the system.

Options: Every day, Selective.

**Wake up hour / Wake up minute**

This item allows you to set the system to wake up at the hr:min specified.

**Wake System duration after shutdown**

When enabled, system will wake up at current time + Increment in minutes(s) after shutdown. When enabled, the related items will appear.

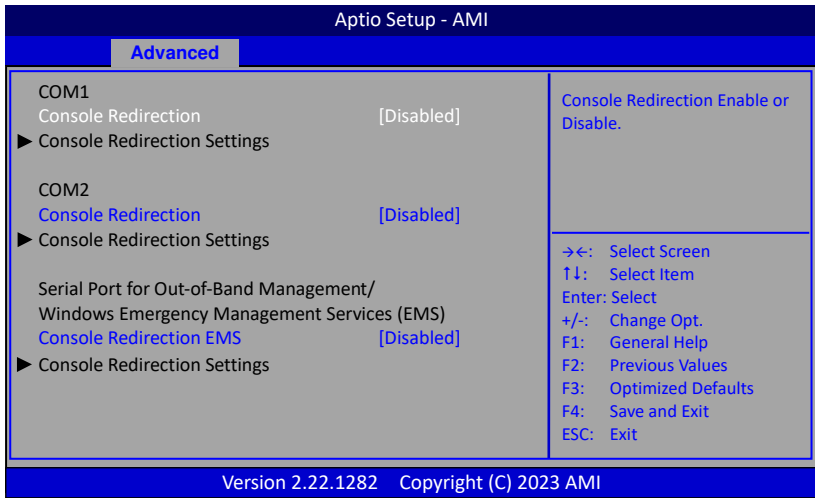
Options: Enabled, Disabled.

**Duration (minute)**

This item allows you to set duration time to wake system.

Options: 1 ~ 30.

► **Serial Port Console Redirection**



**COM1 Console Redirection**

Enable or disable console redirection for COM1. When enabled, the related items will appear.

Options: Enabled, Disabled.

**COM2 Console Redirection**

Enable or disable console redirection for COM2. When enabled, the related items will appear.

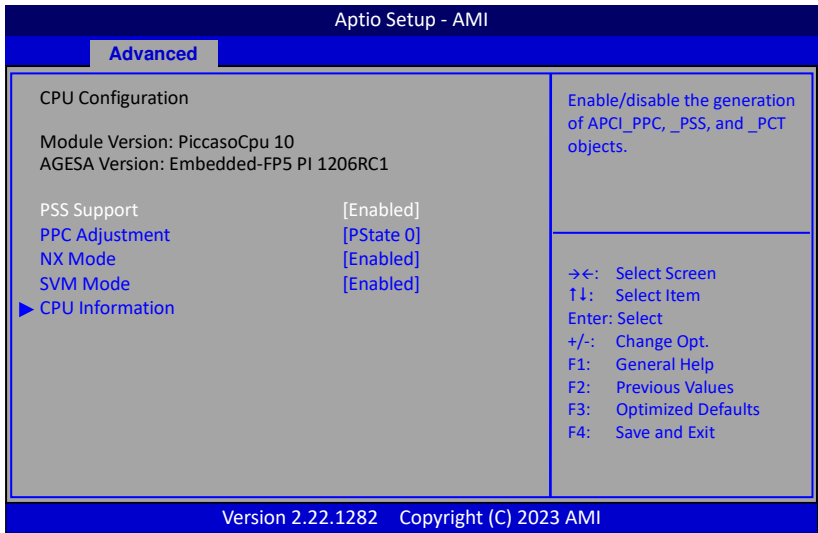
Options: Enabled, Disabled.

**Console Redirection EMS**

Enable or disable console redirection for EMS. When enabled, the related items will appear.

Options: Enabled, Disabled.

► **CPU Configuration**



**PSS Support**

Enable/disable the generation of APCI\_PPC, \_PSS, and \_PCT objects.

Options: Enabled, Disabled.

**PPC Adjustment**

Allows you to adjust \_PPC object.

Options: PState 0, PState 1, PState 2.

**NX Mode**

Enable or disable No-execute page protection function.

Options: Enabled, Disabled.

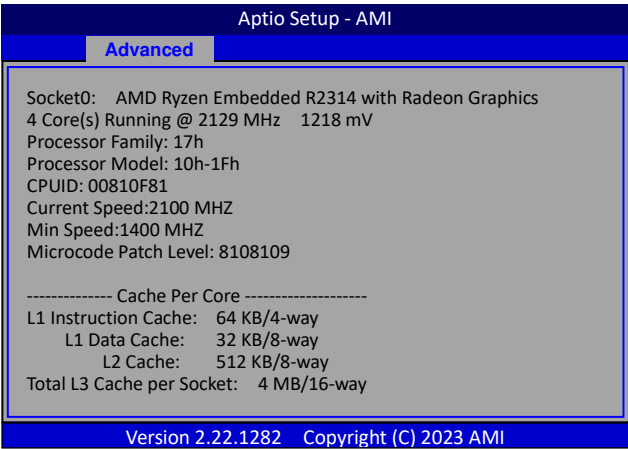
**SVM Mode**

Enables the CPU SVM (Secure Virtual Machine) function.

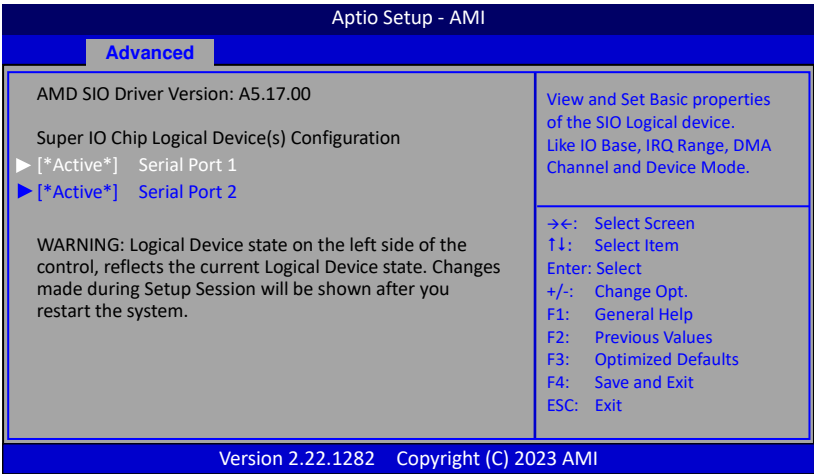
Options: Enabled, Disabled.

► **CPU Information**

Displays current processor information.



► **SIO Configuration**



**[\*Active\*] Serial Port 1/[\*Active\*] Serial Port 2**

View and Set Basic properties of the SIO Logical device. Like IO Base, IRQ Range, DMA Channel and Device Mode.

► **PCI Subsystem Settings**

| Aptio Setup - AMI                |                                                         |
|----------------------------------|---------------------------------------------------------|
| Advanced                         |                                                         |
| PCI Bus Driver Version: A5.01.26 | Value to be programmed into PCI Latency Timer Register. |
| PCI Devices Common Settings:     |                                                         |
| PCI Latency Timer                | [32 PCI Bus Clocks]                                     |
| PCI-X Latency Timer              | [64 PCI Bus Clocks]                                     |
| VGA Palette Snoop                | [Disabled]                                              |
| PERR# Generation                 | [Disabled]                                              |
| SERR# Generation                 | [Disabled]                                              |
| Above 4G Decoding                | [Enabled]                                               |
| SR-IOV Support                   | [Disabled]                                              |
| BME DMA Mitigation               | [Disabled]                                              |
| →←: Select Screen                |                                                         |
| ↑↓: Select Item                  |                                                         |
| Enter: Select                    |                                                         |
| +/-: Change Opt.                 |                                                         |
| F1: General Help                 |                                                         |
| F2: Previous Values              |                                                         |
| F3: Optimized Defaults           |                                                         |
| F4: Save and Exit                |                                                         |
| ESC: Exit                        |                                                         |
| ► PCI Express Settings           |                                                         |
| ► PCI Express GEN 2 Settings     |                                                         |
| ► PCI Hot-Plug Settings          |                                                         |

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**PCI Latency Timer**

Value to be programmed into PCI Latency Timer Register.

Options: 32 PCI Bus Clocks, 64 PCI Bus Clocks, 96 PCI Bus Clocks,  
128 PCI Bus Clocks, 160 PCI Bus Clocks, 192 PCI Bus Clocks,  
224 PCI Bus Clocks, 248 PCI Bus Clocks.

**PCI-X Latency Timer**

Value to be programmed into PCI-X Latency Timer Register.

Options: 32 PCI Bus Clocks, 64 PCI Bus Clocks, 96 PCI Bus Clocks,  
128 PCI Bus Clocks, 160 PCI Bus Clocks, 192 PCI Bus Clocks,  
224 PCI Bus Clocks, 248 PCI Bus Clocks.

**VGA Palette Snoop**

Enable or disable VGA Palette Registers Snooping.

Options: Enabled, Disabled.

**PERR# Generation**

Enable or disable PCI device to generate PERR#.

Options: Enabled, Disabled.

**SERR# Generation**

Enable or disable PCI device to generate SERR#.

Options: Enabled, Disabled.

**Above 4G Decoding**

Enable or disable 64bit capable device to be decoded in above 4G address space (only if system supports 64bit PCI decoding).

Options: Enabled, Disabled.

**SR-IOV Support**

If system has SR-IOV capable PCIe devices, this option enables or disables Single Root IO Virtualization support.

Options: Enabled, Disabled.

**BME DMA Mitigation**

Re-enable bus master attribute disabled during PCI enumeration for PCI bridges after SMM locked.

Options: Enabled, Disabled.

**PCI Express Settings**

**PCI Express GEN 2 Settings**

**PCI Hot-Plug Settings**

These fields are for enable or disable PCI Express Devices related ordering.

► **USB Configuration**

Aptio Setup - AMI

Advanced

USB Configuration

USB Module Version28

USB controllers:  
2 XHCIs

USB Devices:  
1 Keyboard, 1 Mouse

Legacy USB Support[Enabled]

XHCI Hand-off[Enabled]

USB Mass Storage Driver Support[Enabled]

Port 60/64 Emulation[Enabled]

USB Hardware delays and time-outs:

USB transfer time-out[5 sec]

Device reset time-out[10 sec]

Device power-up delay[Auto]

Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLED option will keep USB devices available only for EFI applications.

→←: Select Screen  
↑↓: Select Item  
Enter: Select  
+/-: Change Opt.  
F1: General Help  
F2: Previous Values  
F3: Optimized Defaults  
F4: Save and Exit  
ESC: Exit

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---

### **Legacy USB Support**

Allows you to select legacy support for USB devices.

Enabled: Enables Legacy USB support.

Disabled: Keep USB devices available only for EFI application.

Auto: Disables legacy support if no USB devices are connected.

### **XHCI Hand-off**

This is a workaround for OSeS without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.

Options: Enabled, Disabled.

### **USB Mass Storage Driver Support**

Allows you to enable or disable USB Mass Storage Driver support.

Options: Enabled, Disabled.

### **Port 60/64 Emulation**

Enable I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OSeS.

Options: Enabled, Disabled.

### **USB transfer time-out**

The time-out value for control, bulk, and interrupt transfers.

Options: 1 sec, 5 sec, 10 sec, 20 sec.

### **Device reset time-out**

Sets USB mass storage devices start unit command time-out.

Options: 10 sec, 20 sec, 30 sec, 40 sec.

### **Device power-up delay**

Maximum time the device will take before it properly reports itself to the Host controller. 'Auto' uses default values: for a Root port it is 100ms, for a Hub port the delay is taken from Hub descriptor.

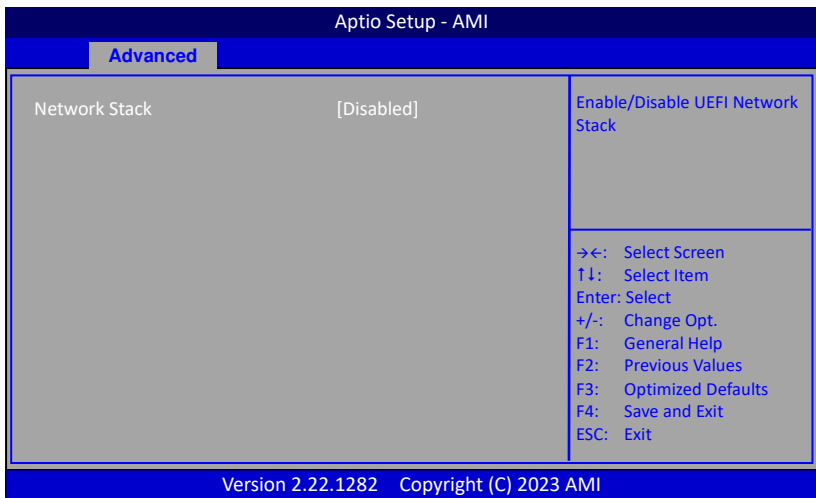
Options: Auto, Manual.

#### **Device power-up delay in seconds**

This item is used to set a wait time in seconds for device power-up delay.

Options: 1 ~ 40.

► **Network Stack Configuration**



**Network Stack**

This item is used for network boot in UEFI mode. When enabled, the related items will appear.

Options: Enabled, Disabled.

**Ipv4 PXE Support**

This item is used to enable or disable the Ipv4 PXE boot support. If disabled, Ipv4 PXE boot option will not be available.

Options: Enabled, Disabled.

**Ipv4 HTTP Support**

This item is used to enable or disable the Ipv4 HTTP boot support. If disabled, Ipv4 HTTP boot option will not be available.

Options: Enabled, Disabled.

**Ipv6 PXE Support**

This item is used to enable or disable the Ipv6 PXE boot support. If disabled Ipv6 PXE boot option will not be available.

Options: Enabled, Disabled.

**Ipv6 HTTP Support**

This item is used to enable or disable the Ipv6 HTTP boot support. If disabled, Ipv6 HTTP boot option will not be available.

Options: Enabled, Disabled.

**PXE boot wait time**

This item is used to set a wait time in seconds for PXE boot. Press ESC key to abort the PXE boot.

Options: 0~5 sec.

**Media detect count**

Number of times presence of media will be checked.

► **CSM Configuration**

| Aptio Setup - AMI                          |                   |                                                                                                                                                                                  |
|--------------------------------------------|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Advanced                                   |                   |                                                                                                                                                                                  |
| Compatibility Support Module Configuration |                   | Enable/Disable CSM Support                                                                                                                                                       |
| CSM Support                                | [Enabled]         |                                                                                                                                                                                  |
| CSM16 Module Version                       | 07.84             |                                                                                                                                                                                  |
| GateA20 Active                             | [Upon Request]    | →←: Select Screen<br>↑↓: Select Item<br>Enter: Select<br>+/-: Change Opt.<br>F1: General Help<br>F2: Previous Values<br>F3: Optimized Defaults<br>F4: Save and Exit<br>ESC: Exit |
| Option ROM Messages                        | [Force BIOS]      |                                                                                                                                                                                  |
| INT19 Trap Response                        | [Immediate]       |                                                                                                                                                                                  |
| HDD Connection Order                       | [Adjust]          |                                                                                                                                                                                  |
| Boot option filter                         | [UEFI and Legacy] |                                                                                                                                                                                  |
| Option ROM execution                       |                   |                                                                                                                                                                                  |
| Network                                    | [Legacy]          |                                                                                                                                                                                  |
| Storage                                    | [Legacy]          |                                                                                                                                                                                  |
| Video                                      | [Legacy]          |                                                                                                                                                                                  |
| Other PCI devices                          | [UEFI]            |                                                                                                                                                                                  |
| Version 2.22.1282 Copyright (C) 2023 AMI   |                   |                                                                                                                                                                                  |

**CSM Support**

This item allows enable or disable the CSM (Compatibility Support Module) configuration.

Options: Enabled, Disabled.

**GateA20 Active**

This feature determines how Gate A20 is used to address memory above 1MB. Upon Request: GA20 can be disabled using BIOS services.

Always: Do not allow disabling GA20.

**Option ROM Message**

Sets display mode for Option ROM.

Force BIOS: To force to a BIOS-compatible output. This will show the option ROM messages.

Keep Current: To keep the current video mode. This will suppress option ROM

messages. Option ROMs requiring interactive inputs may not work properly in this mode.

**INT19 Trap Response**

This item allows BIOS reaction on INT19 trapping by option ROM.

Immediate: Execute the trap right away.

Postponed: Execute the trap during legacy boot.

**HDD Connection Order**

Some OS require HDD handles to adjusted, i.e. OS is installed on drive 80h.

Options: Adjust, Keep.

**Boot option filter**

This option controls what devices system can boot to UEFI or Legacy.

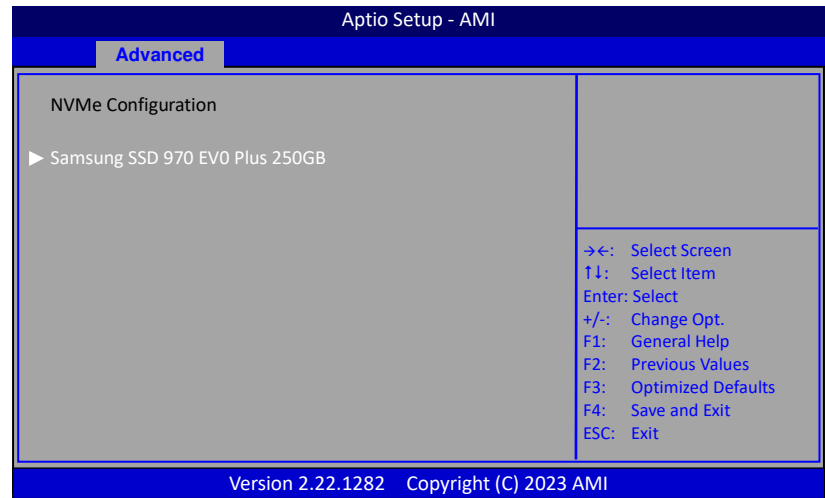
Options: UEFI and Legacy, Legacy only, UEFI only.

**Option ROM execution**

This field controls the execution policy for Network, Storage, Video and other PCI devices.

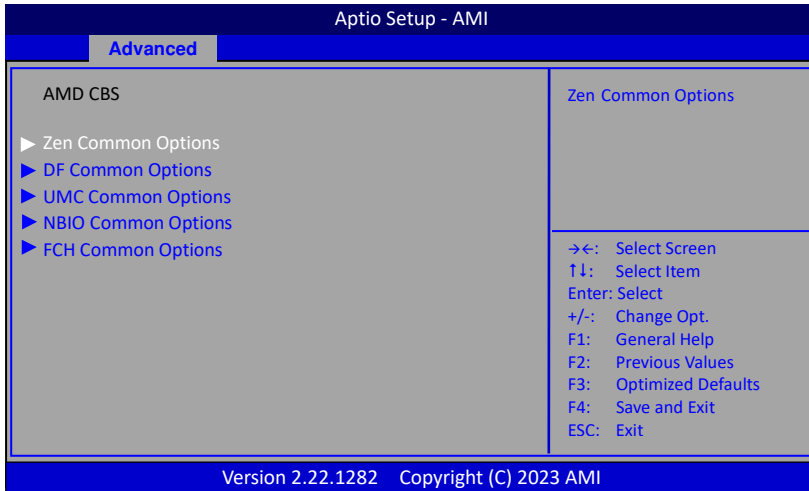
Options: Do not launch, Legacy, UEFI.

► **NVMe Configuration**



This field is displayed the NVMe controller and Drive information.

## ▶ AMD CBS



## ▶ Zen Common Options

### **RedirectForReturnDis**

From a workaround for GCC/C000005 issue for XV Core on CZ A0, setting MSRC001\_1029 Decode Configuration (DE\_CFG) bit 14 [DecfgNoRdrctForReturns] to 1.  
Options: Auto, 1, 0.

### **L2 TLB Associativity**

Allows you set the L2 TLB Associativity. 0 – L2 TLB ways [11:8] are fully associative. 1 – L2 TLB ways [11:8] are 4K only.  
Options: Auto, 1, 0.

### **Platform First Error Handling**

Allows you enable or disable PFEH, clock individual banks, and mask deferred error interrupts from each bank.  
Options: Enabled, Disabled, Auto.

### **Core Performance Boost**

Allows you set the Core Performance Boost.  
Options: Disabled, Auto.

### **Global C-State Control**

Allows you controls IO based C-State generation and DF C-states.  
Options: Enabled, Disabled, Auto.

---

### **Core/Thread Enablement**

Allows you set the Core/Thread Enablement. S3 is NOT SUPPORTED on systems where cores/threads have been removed/disabled.

Options: Disagree, Agree.

### **Streaming Stores Control**

Allows you enable or disable the streaming stores functionality.

Options: Enabled, Disabled, Auto.

### **Enable IBS**

When IBS is enabled, SpecLockMap and Stack Engine are disabled.

Options: Enabled, Disabled, Auto.

### **RPMC Control**

Allows you enable or disable the RPMC function. Auto is Keep default behavior.

Options: Enabled, Disabled, Auto.

## **▶ DF Common Options**

### **DRAM scrub time**

Provide a value that is the number of hours to scrub memory.

Options: Disabled, 1 hour, 4 hours, 8 hours, 16 hours, 24 hours, 48 hours, Auto.

### **Redirect scrubber control**

Allows you set Redirect scrubber control.

Options: Enabled, Disabled, Auto.

### **Disable DF sync flood propagation**

Allows you set sync flood propagation.

Options: Sync flood disabled, Sync flood enabled, Auto.

### **GMI encryption control**

Allows you control GMI link encryption.

Options: Enabled, Disabled, Auto.

### **XGMI encryption control**

Allows you control XGMI link encryption.

Options: Enabled, Disabled, Auto.

### **CC6 memory region encryption**

Allows you control whether or not the CC6 save/restore memory is encrypted.

Options: Enabled, Disabled, Auto.

---

### **Location of private memory regions**

Controls whether or not the private memory regions (PSP, SMU and CC6) are at the top of DRAM or distributed. Note that distributed requires memory on all dies, it will always be at the top of DRAM if some dies don't have memory regardless of this option's setting.

Options: Distributed, Consolidated, Auto.

### **System probe filter**

Controls whether or not the probe filter is enabled. Has no effect on parts where the probe filter is fuse disabled.

Options: Enabled, Disabled, Auto.

### **Memory interleaving**

Controls fabric level memory interleaving. Note that channel, die and socket has requirements on memory populations and it will be ignored if the memory doesn't support the selected option.

Options: None, Channel, Die, Socket, Auto.

### **Memory interleaving size**

Controls the memory interleaving size. This determines the starting address of the interleave (bit 8, 9, 10, or 11).

Options: 256 Bytes, 512 Bytes, 1 KB, 2KB, Auto.

### **Channel interleaving hash**

Controls whether or not the address bits are hashed during channel interleave mode. This field should not be used unless the interleaving is set to channel and the interleaving size is 256 or 512 bytes.

Options: Enabled, Disabled, Auto.

### **DF C-state control**

Allow you enable or disable DF C-state.

Options: Enabled, Disabled, Auto.

### **XGMI DLWM control**

Controls the XGMI dynamic link width management feature.

Options: Enabled, Disabled, Auto.

### **Freeze DF module queues on error**

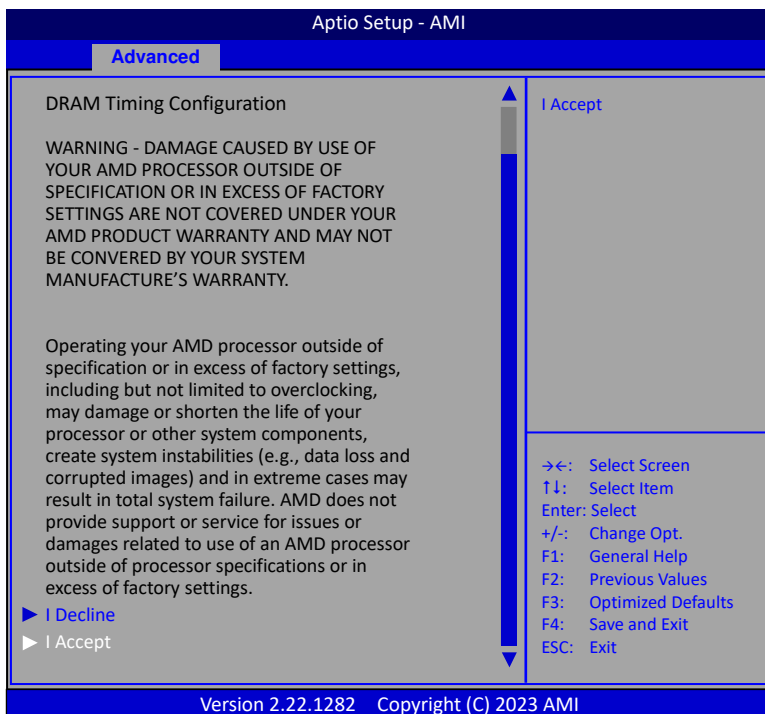
Controls the Freeze DF module queues on error feature.

Options: Enabled, Disabled, Auto.

## 🔧 UMC Common Options

### DDR4 Common Options

#### DRAM Timing Configuration



Select "I Accept" item to enter the overclock function.

#### **Overclock**

When set to "Enabled", allow you to individually set overclock parameters.

Options: Auto, Enabled.

#### **Memory Clock Speed**

Recommend to select and follow below items option only.

1200MHz → 2400MHz

1600MHz → 3200MHz

#### **Note:**

Please attention DRAM timing configuration "WARNING" description. If there is no boot after setting, please to do CMOS clear.

---

## **DRAM Control Configuration**

### **DRAM Power Options**

#### **Power Down Enable**

Allows you to enable or disable DDR power down mode.

Options: Enabled, Disabled, Auto.

#### **Gear Down Mode**

Allows you to enable or disable gear down mode.

Options: Enabled, Disabled, Auto.

#### **Data Mask**

Allows you to enable or disable data mask.

Options: Enabled, Disabled, Auto.

## **CAD Bus Configuration**

### **CAD Bus Timing User Controls**

Drive strength on CAD bus signals to Auto or Manual.

Options: Manual, Auto.

### **CAD Bus Timing User Controls**

Specify the mode for drive strength to Auto or Manual.

Options: Manual, Auto.

## **Data Bus Configuration**

### **Data Bus Configuration User Controls**

Specify the mode for drive strength to Auto or Manual.

Options: Manual, Auto.

## **Common RAS**

### **Data Poisoning**

Enable or disable data poisoning: UMC\_CH::EccCtrl[UcFatalEn]

UMC\_CH::EccCtrl[WrrEccEn] should be enabled/disabled together.

Options: Enabled, Disabled, Auto.

### **ECC Configuration**

#### **DRAM ECC Symbol Size**

Use this option to select the DRAM ECC Symbol Size.

Options: x4, x8, Auto.

#### **DRAM ECC Enable**

Use this option to enable/disable DRAM ECC. Auto will set ECC to enable.

Options: Enabled, Disabled, Auto.

---

### **Disable Memory Error Injection**

Use this option to control Disable Memory Error Injection.

Options: False, True.

## **DRAM Memory Mapping**

### **Chip select Interleaving**

Interleave memory blocks across the DRAM chip selects for node 0.

Options: Disabled, Auto.

### **BankGroupSwap**

Use this option to control BankGroupSwap.

Options: APU, CPU, Disabled, Auto.

### **BankGroupSwapAlt**

Use this option to control BankGroupSwapAlt.

Options: Enabled, Disabled, Auto.

### **Address Hash Bank**

Use this option to enable or disable bank address hashing.

Options: Enabled, Disabled, Auto.

### **Address Hash CS**

Use this option to enable or disable CS address hashing.

Options: Enabled, Disabled, Auto.

## **Memory MBIST**

### **MBIST Enable**

Use this option to enable or disable Memory MBIST.

Options: Enabled, Disabled, Auto.

## **► NBIO Common Options**

### **GFX Configuration**

#### **Integrated Graphics Controller**

Use this option to enable or disable Integrated Graphics Controller.

Options: Disabled, Force, Auto.

#### **UMA Mode**

Allows you to select the UMA mode.

Options: Auto, UMA\_SPECIFIED, UMA\_AUTO.

#### **UMA Frame buffer Size**

This item will only appear when "UMA Mode" item is set to "UMA\_SPECIFIED" option. It controls the amount of system memory that is allocated to the integrated graphics

---

processor.

Options: Auto, 64M, 80M, 96M, 128M, 256M, 384M, 512M, 768M, 1G, 2G, 3G, 4G, 8G, 16G.

### **Display Resolution**

This item will only appear when "UMA Mode" item is set to "UMA\_AUTO" option. It allows you select the display resolution.

Options: 1920x1080 and below, 2560x1600, 3840x2160, Auto.

### **UMA Version**

Allows you to select the UMA legacy version.

Options: Legacy, Non-Legacy, Hybrid Secure, Auto.

### **UMA Above 4G**

If requested UMA frame buffer size can't be fit under 4GB or the system has enough available memory above 4GB, this option may be set to TURE to allow UMA frame buffer size to be allocated successfully.

Options: Disabled, Enabled, Auto

### **DP/HDMI Audio**

Allows you to enable or disable the Integrated HD Audio Controller.

Options: Disabled, Enabled, Auto

## **NB Configuration**

### **IOMMU**

This item allows you to enable or disable the IOMMU (Input/Output Memory Management Unit).

Options: Disabled, Enabled, Auto.

## **PCIe Configuration**

### **PSPP Policy**

This item allows you to select PCIe speed power policy.

Options: Disabled, Performance, Balanced, Power Saving, Auto.

## **System Configuration**

This item allows you to select the System Configuration. Not all TDP/System configurations listed can be applied: Check the Infrastructure Roadmap Document on DevHub (Infrastructure tab). The Auto configuration will be applied in case an unsupported system configuration (lower or upper out of bound) is selected. The Auto configuration is the

---

upper/highest Embedded system configuration supported for an Embedded Rayzen part.

Options:

12W POR Configuration

15W POR Configuration

25W POR Configuration

35W POR Configuration

Auto.

---

*Warning: Select System Configuration may cause the system to hang, as some System Configuration may not be supported by your OPN.*

---

### **System Temperature Tracking**

This item allows you to select the System Temperature Tracking.

[0=disabled; 1= enabled]

Options: Auto, Disabled, Enabled.

## **► FCH Common Options**

### **AC Power Loss Options**

#### **Ac Loss Control**

Enables your computer to automatically restart or return to its last operating status after power returns from a power failure.

Options: Always Off, Always On, Previous.

### **I2C Configuration Options**

#### **I2C 0 Enable / I2C 1 Enable / I2C 2 Enable**

This item allows you to select the I2C Configuration.

Options: Auto, Disabled, Enabled.

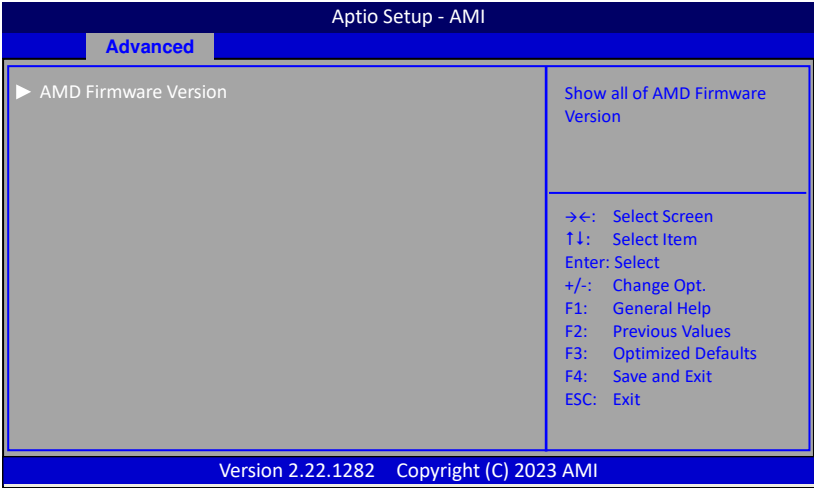
### **System Control**

#### **Toggle All PwrGood On Cf9**

This item allows you to select the Toggle All PwrGood On Cf9 control.

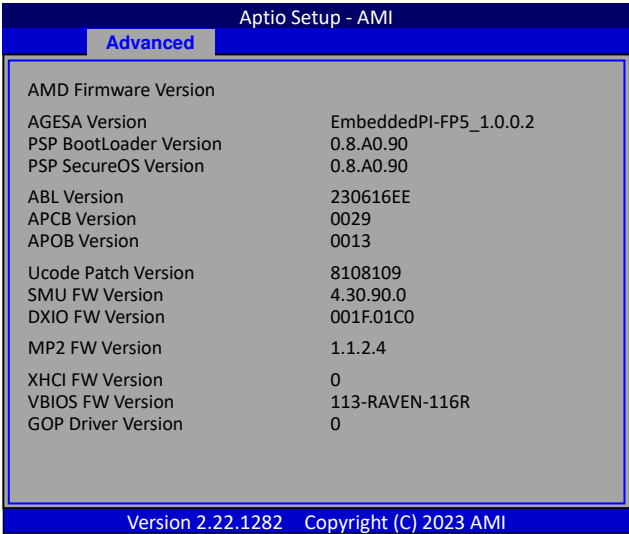
Options: Auto, Disabled, Enabled.

► **AMD PBS**



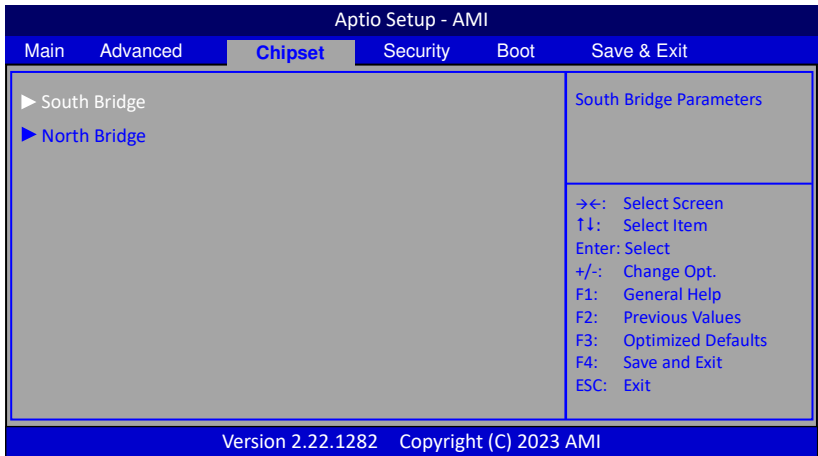
► **AMD Firmware Version**

Show all of AMD Firmware Version.

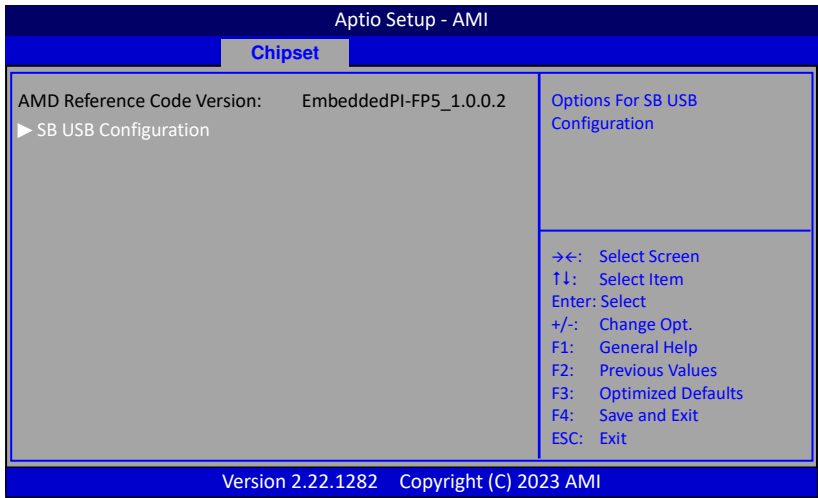


### 3-5 Chipset Menu

The chipset menu items allow you to change the advanced chipset settings. Press <Enter> to display the sub-menu.



► **South Bridge**



► **SB USB Configuration**

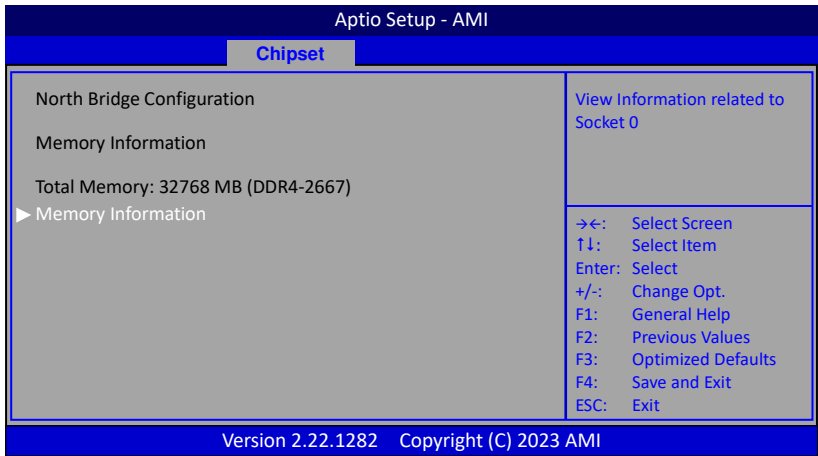
**USB2.0 Port (Black, Top) / USB2.0 Port (Black, Bottom) /  
USB3.2 Port (Blue, Top) / USB3.2 Port (Blue, Bottom) /**

### USB3.2 TYPE-C Port / USB2.0 HUB

Allows you to enable or disable USB ports.

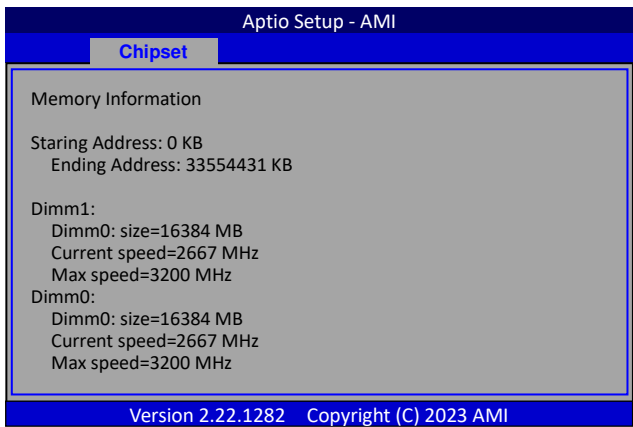
Options: Enabled, Disabled.

► **North Bridge**



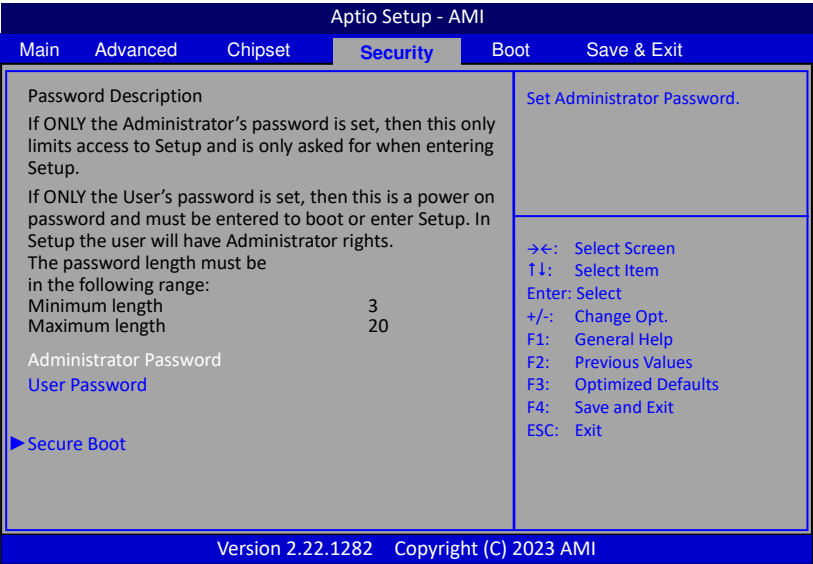
► **Memory Information**

Displays the memory related information.



### 3-6 Security Menu

The Security menu allows you to change the system security settings.



#### Administrator Password

This function is used to set, change or delete the Administrator password. If there is already a password installed, the system asks for this first. To clear a password, simply enter nothing and acknowledge by pressing Return. To set a password, enter it twice and acknowledge by pressing Return. The password must be 3 to 20 characters long.

#### User Password

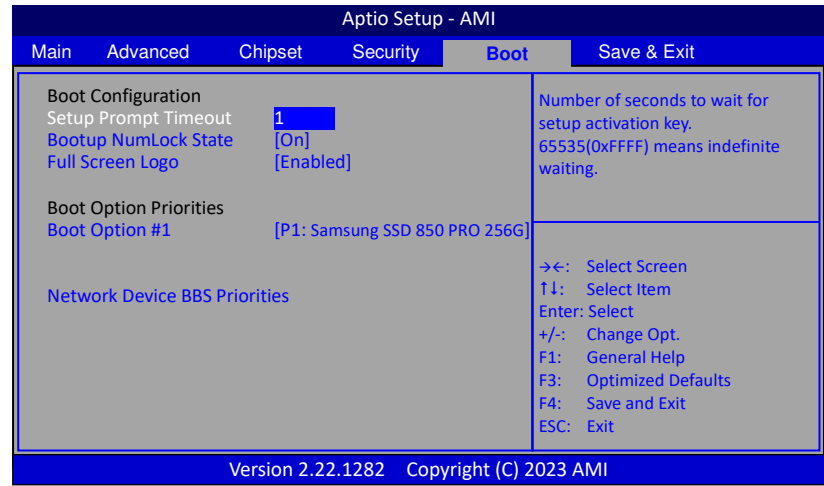
This function is used to set, change or delete the User password. If there is already a password installed, the system asks for this first. To clear a password, simply enter nothing and acknowledge by pressing Return. To set a password, enter it twice and acknowledge by pressing Return. The password must be 3 to 20 characters long.

#### Secure Boot

Secure Boot feature is Active if Secure Boot is Enabled. Platform Key (PK) is enrolled and the system is in user mode. The mode change requires platform reset.

# 3-7 Boot Menu

The Boot menu is used to configure the boot settings and the boot priority.



## Setup Prompt Timeout

This is used to set an additional time the POST should wait for the operator to press the key to enter setup. The time is entered in seconds.

## Bootup NumLock State

Selects the state of the keyboard’s Numlock function after POST.

Options: On, Off.

## Full Screen Logo

This item allows you to enable or disable the full screen logo display feature.

Options: Enabled, Disabled.

## Boot Option Priorities

These items specify the boot device priority sequence of the available devices.

The number of device items that appears on the screen depends on the number of devices installed in the system.

## Hard Drive BBS Priorities

Allows you to configure the boot order for a specific Hard Drive device class.

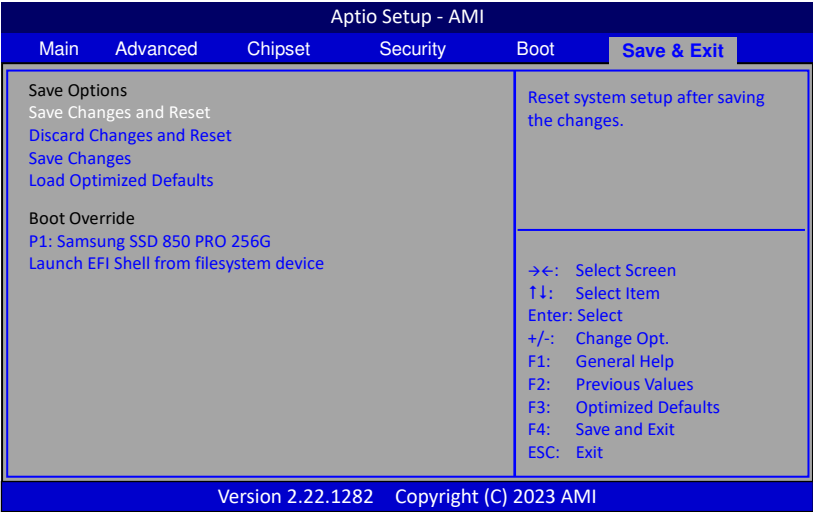
## Network Device BBS Priorities

Allows you to configure the boot order for a specific Network device class.

---

# 3-8 Save & Exit Menu

The Save & Exit menu allows you to load the optimal default values for BIOS, and save or discard your changes to the BIOS items.



## Save Options

Allows you to save the options you made.

### Save Changes and Reset

This resets system after saving the changes.

### Discard Changes and Reset

This resets system without saving the changes.

### Save Changes

Allows you to save the changes you made.

### Load Optimized Defaults

The Load default values are the factory settings of this motherboard.

## Boot Override

This group of functions includes a list, each of them corresponding to one device within the boot order. Select a drive to immediately boot that device regardless of the current boot order.

### Launch EFI Shell from filesystem device

Attempts to launch EFI Shell application (Shellx64.efi) form one of the available filesystem devices.

---

## **Chapter 4    Firmware and Driver Installation**

After the operating system has been installed, you need to install the software and drivers for this mainboard. The OSPI firmware may also need to be updated.

Please visit <http://www.sapphiretech.com> or <http://www.amd.com> to download the latest driver.

---

## **Chapter 5 Chassis Installation**

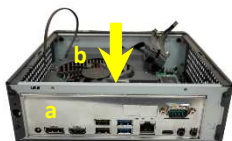
Follow the instructions below to install the mainboard into the chassis.



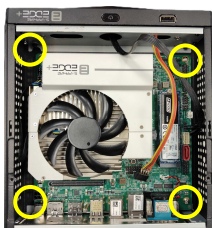
Remove the 2 screws on back of chassis to open the cover of chassis.



Remove the 2 screws of SATA bracket to take out the SATA bracket.



- a. Place the I/O shield on back of chassis first.
- b. Identify the I/O connector location and install the mainboard into the chassis.



Fasten mainboard into the chassis with 4 accompanied screws of chassis.



- a. Connect the power button cable to front panel header (CFP1) of mainboard. Need to be connected to the corresponding headers separately.
- b. Connect the USB cable to USB2.0 header (USB2-A) of mainboard.



Fasten SATA bracket to chassis with 2 screws of SATA bracket.



Fasten chassis cover to chassis with 2 screws of chassis.  
The system installation is complete.

---

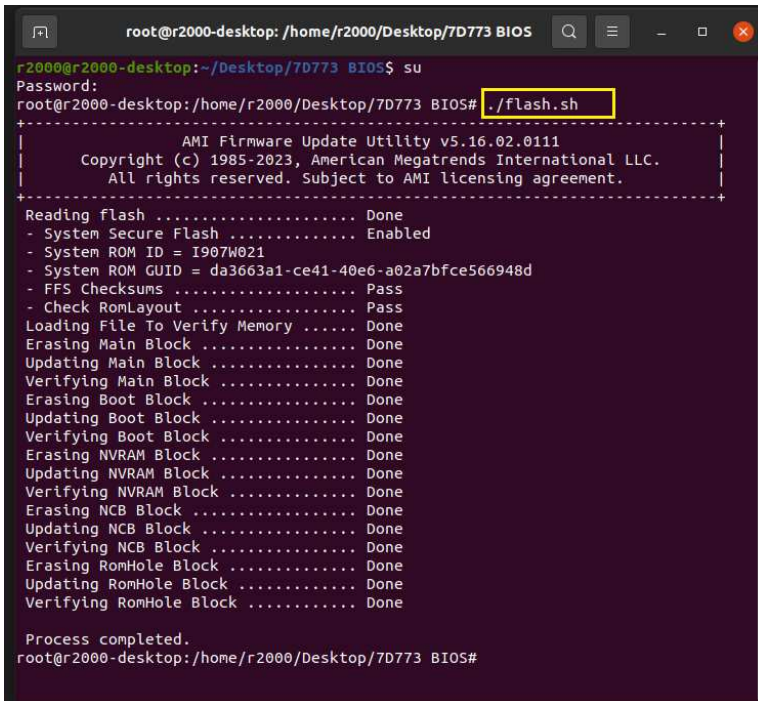
## Appendix A: BIOS Update

Please refer the following steps for BIOS update.

1. Please download the latest BIOS version from this link.  
[www.sappphire.com/xxxxxxxxxxxxxx](http://www.sappphire.com/xxxxxxxxxxxxxx)
2. After downloading the compressed file, there are four files upon extracting the archive.

|                                                                                                |                   |        |          |
|------------------------------------------------------------------------------------------------|-------------------|--------|----------|
|  afulnx_64    | 2024/2/2 上午 07:11 | 檔案     | 1,160 KB |
|  flash.sh     | 2024/2/2 上午 07:11 | SH 檔案  | 1 KB     |
|  I907W021.rom | 2024/2/2 上午 07:11 | ROM 檔案 | 8,192 KB |
|  readme       | 2024/2/2 上午 07:11 | 文字文件   | 6 KB     |

3. Open a terminal window in this folder and execute the command #  
sudo ./flash.sh
4. Update completed, as shown in the following picture.

A terminal window titled 'root@r2000-desktop: /home/r2000/Desktop/7D773 BIOS' is shown. The user has entered 'su' and then './flash.sh'. The output displays the AMI Firmware Update Utility v5.16.02.0111, copyright 1985-2023, American Megatrends International LLC. The update process is shown as a series of steps, each with a progress indicator (dots) and a status (Done, Enabled, Pass). The steps include: Reading flash, System Secure Flash, System ROM ID, System ROM GUID, FFS Checksums, Check RomLayout, Loading File To Verify Memory, Erasing Main Block, Updating Main Block, Verifying Main Block, Erasing Boot Block, Updating Boot Block, Verifying Boot Block, Erasing NVRAM Block, Updating NVRAM Block, Verifying NVRAM Block, Erasing NCB Block, Updating NCB Block, Verifying NCB Block, Erasing RomHole Block, Updating RomHole Block, and Verifying RomHole Block. The process is completed, and the prompt returns to 'root@r2000-desktop: /home/r2000/Desktop/7D773 BIOS#'.

```
root@r2000-desktop: /home/r2000/Desktop/7D773 BIOS
r2000@r2000-desktop:~/Desktop/7D773 BIOS$ su
Password:
root@r2000-desktop: /home/r2000/Desktop/7D773 BIOS# ./flash.sh
+-----+
|              AMI Firmware Update Utility v5.16.02.0111              |
| Copyright (c) 1985-2023, American Megatrends International LLC.     |
| All rights reserved. Subject to AMI licensing agreement.            |
+-----+
Reading flash ..... Done
- System Secure Flash ..... Enabled
- System ROM ID = I907W021
- System ROM GUID = da3663a1-ce41-40e6-a02a7bfce566948d
- FFS Checksums ..... Pass
- Check RomLayout ..... Pass
Loading File To Verify Memory ..... Done
Erasing Main Block ..... Done
Updating Main Block ..... Done
Verifying Main Block ..... Done
Erasing Boot Block ..... Done
Updating Boot Block ..... Done
Verifying Boot Block ..... Done
Erasing NVRAM Block ..... Done
Updating NVRAM Block ..... Done
Verifying NVRAM Block ..... Done
Erasing NCB Block ..... Done
Updating NCB Block ..... Done
Verifying NCB Block ..... Done
Erasing RomHole Block ..... Done
Updating RomHole Block ..... Done
Verifying RomHole Block ..... Done

Process completed.
root@r2000-desktop: /home/r2000/Desktop/7D773 BIOS#
```

---

## **Appendix B: Qualified Vendors List**

### **Qualified Vendors List for Memory modules**

#### **➤ DDR4 2133 Memory modules**

| Vendor    | Module P/N         | Size | Component       | Voltage | DIMM socket support |        |
|-----------|--------------------|------|-----------------|---------|---------------------|--------|
|           |                    |      |                 |         | 1 DIMM              | 2 DIMM |
| ADATA     | AD4S2133W4G15-BSSD | 4GB  | K4A4G085WD      | 1.2V    | ✓                   | ✓      |
| GeIL      | GS44GB2133C15SC    | 4GB  | GeIL 512X8DDR4  | 1.2V    | ✓                   | ✓      |
| GOODRAM   | GR4S4GB213S8C      | 4GB  | K4A4G085WE      | 1.2V    | ✓                   | ✓      |
| Innodisk  | M4S0-4GSSNCRG      | 4GB  | K4A4G085WD      | 1.2V    | ✓                   | ✓      |
| SMART     | SH5126SO451851-HA  | 4GB  | H5AN4G8NAFR TFC | 1.2V    | ✓                   | ✓      |
| Transcend | TS512M5H64V1H      | 4GB  | K4A4G085WD      | 1.2V    | ✓                   | ✓      |
| Transcend | TS512M5H72V1H ECC  | 4GB  | K4A4G085WD      | 1.2V    | ✓                   | ✓      |
| TEAM      | TED44G2133C15-SBK  | 4GB  | T4D5128HT-21    | 1.2V    | ✓                   | ✓      |
| GeIL      | GS48GB2133C15SC    | 8GB  | GeIL 512X8DDR4  | 1.2V    | ✓                   | ✓      |
| Innodisk  | M4S0-8GSSOCRG      | 8GB  | K4A4G085WD      | 1.2V    | ✓                   | ✓      |
| SMART     | SH1026SO451851-HA  | 8GB  | H5AN4G8NAFR TFC | 1.2V    | ✓                   | ✓      |
| SMART     | SH1026SO410851-SB  | 8GB  | K4A8G08 5WB     | 1.2V    | ✓                   | ✓      |
| Transcend | TS1GSH64V1H        | 8GB  | K4A4G08 5WD     | 1.2V    | ✓                   | ✓      |
| SMART     | SH2046SO410851-HM  | 16GB | H5AN8G8NMFR TFC | 1.2V    | ✓                   | ✓      |

#### **➤ DDR4 2400 Memory modules**

| Vendor   | Module P/N            | Size | Component       | Voltage | DIMM socket support |        |
|----------|-----------------------|------|-----------------|---------|---------------------|--------|
|          |                       |      |                 |         | 1 DIMM              | 2 DIMM |
| SMART    | SH5126SO451672-HA     | 4GB  | H5AN8G8NAFR UHC | 1.2V    | ✓                   | ✓      |
| SMART    | SH5127SO451872-HA ECC | 4GB  | H5AN4G8NAFR UHC | 1.2V    | ✓                   | ✓      |
| GOODRAM  | GR4S4G240S8C-SERC     | 4GB  | SEC 819 K4A4G08 | 1.2V    | ✓                   | ✓      |
| Kingston | CBD24D457S8MB-4       | 4GB  | 7CB75 D9TGG     | 1.2V    | ✓                   | ✓      |
| SAMSUNG  | M471A5244CB0-CRC      | 4GB  | SEC 801 K4A8G16 | 1.2V    | ✓                   | ✓      |
| GOODRAM  | GR4S8G240S8C-SBRC     | 8GB  | SEC 731 K4A8G08 | 1.2V    | ✓                   | ✓      |
| Kingston | CBD24D457S8MB-8       | 8GB  | 6RB77 D9TGG     | 1.2V    | ✓                   | ✓      |
| Kingston | CBD24D457S8ME-8       | 8GB  | 7QE75 D9VPP     | 1.2V    | ✓                   | ✓      |
| Kingston | KVR24S17S8/8          | 8GB  | 7SE75 D9VPP     | 1.2V    | ✓                   | ✓      |
| SMART    | SH1026SO410872-HA     | 8GB  | H5AN8G8NAFR UHC | 1.2V    | ✓                   | ✓      |
| SMART    | SH2046SO410872-HM     | 16GB | H5AN8G8NAFR UHC | 1.2V    | ✓                   | ✓      |
| Kingston | KTL-TN424E/16GB ECC   | 16GB | H5AN8G8NAFR UHC | 1.2V    | ✓                   | ✓      |

➤ **DDR4 2666 Memory modules**

| Vendor    | Module P/N           | Size | Component                   | Voltage | DIMM socket support |        |
|-----------|----------------------|------|-----------------------------|---------|---------------------|--------|
|           |                      |      |                             |         | 1 DIMM              | 2 DIMM |
| TEAMGROUP | TED44G2666C19-SBK    | 4GB  | Team Elite<br>TD5128KT-266  | 1.2V    | ✓                   | ✓      |
| SMART     | SH1026SO410893-SC    | 8GB  | SWT0A10805383FC175          | 1.2V    | ✓                   | ✓      |
| SAMSUNG   | M471A1K43CB1-CTD     | 8GB  | SEC 843 K4A8608 5WC<br>BCTD | 1.2V    | ✓                   | ✓      |
| KINGSTON  | KVR26S19D8/32        | 32GB | Micron ODB45 D9XPF          | 1.2V    | ✓                   | ✓      |
| Micron    | MTA16ATF4G64HZ-2G6B2 | 32GB | Micron 9FB45 D9XPF          | 1.2V    | ✓                   | ✓      |

➤ **DDR4 2933 Memory modules**

| Vendor   | Module P/N       | Size | Component   | Voltage | DIMM socket support |        |
|----------|------------------|------|-------------|---------|---------------------|--------|
|          |                  |      |             |         | 1 DIMM              | 2 DIMM |
| Kingston | HX429S17IB2K2/16 | 8GB  | 7XE75 D9VPP | 1.2V    | ✓                   | ✓      |

➤ **DDR4 3200 Memory modules**

| Vendor    | Module P/N           | Size | Component                  | Voltage | DIMM socket support |        |
|-----------|----------------------|------|----------------------------|---------|---------------------|--------|
|           |                      |      |                            |         | 1 DIMM              | 2 DIMM |
| * GOODRAM | GR4S4G320S8C-SERC    | 4GB  | SEC 816<br>K4A4G085WE BCRC | 1.2V    | ✓                   | ✓      |
| Micron    | MTA4ATF51264HZ-3G2E1 | 4GB  | 7ZE75 D9WFJ                | 1.2V    | ✓                   | ✓      |
| Micron    | MTA8ATF1G64HZ-3G2E1  | 8GB  | 7XE75 D9WFL                | 1.2V    | ✓                   | ✓      |
| Kingston  | HX432S20IB2K2/16     | 8GB  | 7XE75 D9VPP                | 1.2V    | ✓                   | ✓      |
| * Apacer  | AS08GGB32CLYBGD      | 8GB  | SEC 819 K4A8G08            | 1.2V    | ✓                   | ✓      |

\* The default recognized clock is not 3200MHz, running at 3200MHz requires manual configuration in BIOS. (Advanced > AMD CBS > UMC Common Options > DDR4 Common Options > DRAM Timing Configuration > Overclock > Memory Clock Speed)

## Qualified Vendors List for SSD

### ➤ M.2 SSD

| Vander                  | Model / PN                       | Interface     | Capacity |
|-------------------------|----------------------------------|---------------|----------|
| 2280 Form factor <NVMe> |                                  |               |          |
| ADATA                   | XPG GAMMIX S70 BLADE             | PCIe Gen 4 x4 | 1TB      |
| Kingston                | NV2 SNV2S250G                    | PCIe Gen 4 x4 | 250GB    |
| Samsung                 | PM9B1 MZ-VL41T00                 | PCIe Gen 4 x4 | 1TB      |
| Teamgroup               | T-FORCE TMBFPL250G               | PCIe Gen 4 x4 | 250GB    |
| Kingston                | KC1000 SKC1000/240G NVMe         | PCIe Gen 3 x4 | 240GB    |
| Kingston                | KC2500 SKC2500M8250G             | PCIe Gen 3 x4 | 250GB    |
| PLEXTOR                 | PX-128M8PeGN                     | PCIe Gen 3 x4 | 128GB    |
| Samsung                 | 970 EVO Plus MZ-V7S250           | PCIe Gen 3 x4 | 250GB    |
| Samsung                 | 970 PRO MZ-V7P512                | PCIe Gen 3 x4 | 512GB    |
| Toshiba                 | KXG50ZNV256G                     | PCIe Gen 3 x4 | 256GB    |
| Western Digital         | SN720 SDAPNTW-256G-1016          | PCIe Gen 3 x4 | 256GB    |
| Kingston                | A1000 SA1000M8/480G              | PCIe Gen 3 x2 | 480GB    |
| LITEON                  | PP3-8D128                        | PCIe Gen 3 x2 | 128GB    |
| 2280 Form factor <SATA> |                                  |               |          |
| BIWIN                   | G6312 CNF82DS 1805-128           | SATA          | 128GB    |
| Crucial                 | CT128M550SSD4                    | SATA          | 128GB    |
| Intel                   | SSDSCGW080A4                     | SATA          | 80GB     |
| innodisk                | M.2 (S80) 3TE7 DEM28-64GDK1EC1DF | SATA          | 64GB     |
| Intel                   | SSDSCGW080A4                     | SATA          | 80GB     |
| Kingston                | SUV500M8/240G                    | SATA          | 240GB    |
| Micron                  | 1100 MTFDDAV256TBN               | SATA          | 256GB    |
| Micron                  | 1100 MTFDDAV512TBN               | SATA          | 512GB    |
| PLEXTOR                 | PX-128M6G-2280                   | SATA          | 128GB    |
| SanDisk                 | Z400S SD8SNAT-128G-1002          | SATA          | 128GB    |
| SanDisk                 | Z400S SD8SNAT-256G-1002          | SATA          | 256GB    |
| SanDisk                 | X400 SD8SN8U-512G-1122           | SATA          | 512GB    |
| Samsung                 | MZ-NLN128C                       | SATA          | 128GB    |
| Samsung                 | MZ-N5E250                        | SATA          | 250GB    |
| Western Digital         | WDS120G1G0B-00RC30               | SATA          | 120GB    |

### ➤ 2.5" SSD

| Vander    | Model / PN            | Interface | Capacity |
|-----------|-----------------------|-----------|----------|
| ADVANTECH | SQF-S25M8-128G-S8C    | SATA      | 128GB    |
| ADATA     | S510 AS510S3-60GB     | SATA      | 60GB     |
| LITEON    | PH6-CE120G            | SATA      | 120GB    |
| Intel     | SSDSC2CW120A3         | SATA      | 120GB    |
| Kingston  | SVP100S264G           | SATA      | 64GB     |
| Kingston  | SHF37A/120GG          | SATA      | 120GB    |
| Kingston  | SUV500/240G           | SATA      | 240GB    |
| Micron    | M500 MTFDDAK120MAV    | SATA      | 120GB    |
| Micron    | M510 MTFDDAK256MAZ    | SATA      | 256GB    |
| SanDisk   | X110 SD6SB1M064G1022I | SATA      | 64GB     |
| SanDisk   | Z400s SD8SBAT-128G    | SATA      | 128GB    |
| SanDisk   | Z400s SD8SBAT-256G    | SATA      | 256GB    |
| Samsung   | 850 PRO MZ-7KE256     | SATA      | 256GB    |

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# Qualified Vendors List for WIFI+BT

| Vander   | Model                  |
|----------|------------------------|
| Intel    | AX210 WiFi 6E          |
| Intel    | 9260NGW                |
| Intel    | 8260NGW                |
| Intel    | 3165NGW                |
| MediaTek | MT7922 WIFI-6E (RZ616) |
| Realtek  | RTL8852BE              |

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## Appendix C: Expansion Board & Connector

### Expansion Connector

The expansion connector is high-speed interface for specific peripherals such as cameras or high speed networking. The signals and pin numbers of connector are provided in the following Table.

| Type      | Signal                                                       | Count              |
|-----------|--------------------------------------------------------------|--------------------|
| GTYP      | High Speed transceivers<br>GTYP x4 Tx/Rx data lines + RefClk | 20 (10 diff-pairs) |
| XPIO      | User configurable XPIO                                       | 54 (27 diff-pairs) |
| HDIO      | User configurable HDIO                                       | 22                 |
| XPIO VCCO | User XPIO bank supply voltage                                | 2                  |
| HDIO VCCO | User HDIO bank supply voltage                                | 2                  |
| PWR_EN    | VCCO power sequence control                                  | 1                  |
| 1-Wire    | Board-ID 1-Wire PROM                                         | 1                  |
| 3V3       | 3.3V supply to daughtercard                                  | 4                  |

### Connector Power

The expansion connector includes three power supplies for providing user flexibility in the definition of the FPGA I/O rails as well as providing power to the daughtercard without requiring a separate cable. The expansion connector power pins are described below table

| Connector Power | Source → Sink             | Rating           |
|-----------------|---------------------------|------------------|
| 3V3             | Base board → Daughtercard | 3.3V @ 1A        |
| XPIO_VCCO       | Daughtercard → Base board | 1.0-1.5V @ 500mA |
| HDIO_VCCO       | Daughtercard → Base board | 1.8-3.3V @ 500mA |

#### ➤ Absolute Maximum Ratings

| Symbol    | Description                             | Min   | Max   |
|-----------|-----------------------------------------|-------|-------|
| VCCO_XPIO | XPIO bank 7# output driver power supply | -0.5V | 1.65V |
| VCCO_HDIO | HDIO bank 3# output driver power supply | -0.5V | 3.63V |

#### ➤ Recommended Operating Conditions

| Symbol    | Description                                                                                       | Min    | Typ | Max    |
|-----------|---------------------------------------------------------------------------------------------------|--------|-----|--------|
| VCCO_XPIO | XPIO bank 7# output driver power supply<br>Includes VCCO of 1.0V, 1.1V, 1.2V, 1.35V, 1.5V at ±5%  | 0.950V | -   | 1.575V |
| VCCO_HDIO | HDIO bank 3# output driver power supply<br>Includes VCCO of 1.8V, 2.5V at ±5%, and 3.3V at +3/-5% | 1.710V | -   | 3.4V   |

## Power Enable (VCC\_CARD\_EN)

A power enable (VCC\_CARD\_EN) signal is routed from the Versal device to the expansion card to be used by the local expansion card local power supplies. This signal used to gate the HDIO\_VCCO and XPIO\_VCCO power supplies. The HDIO\_VCCO and XPIO\_VCCO power supplies should remain low until the PWR\_EN signal goes high.

## 1-Wire ID(LPD\_MIO4\_GPIO)

The 1-Wire interface is to be used to implement an expansion card ID mechanism. A 1-wire compliant EEPROM is to be implemented on the expansion card which will capture board name and revision. This information can then be used by the Versal device to ensure PL bitstream to expansion card alignment.

The interface is powered through its I/O pin which will be connected to the 1.8V MIO through a pull-up resistor. An example device is the Microchip AT21CS01/AT21CS11.

## DC Input and Output Levels

### ➤ Operating Conditions

| Symbol        | Description           | Min    | Typ   | Max    |
|---------------|-----------------------|--------|-------|--------|
| VCC_CARD_EN   | PSIO BANK5# PMC MIO31 | 1.71V  | 1.8V  | 1.89V  |
| LPD_MIO4_GPIO | PSIO BANK5# LPD MIO4  | 1.71V  | 1.8V  | 1.89V  |
| GTP           | GTP transceiver       | 1.164V | 1.2V- | 1.236V |

### ➤ PSIO BANK : Input and Output Levels

| I/O<br>Standard | V <sub>IL</sub> |        | V <sub>IH</sub> |        | V <sub>OL</sub> | V <sub>OH</sub> | I <sub>OL</sub> | I <sub>OH</sub> |
|-----------------|-----------------|--------|-----------------|--------|-----------------|-----------------|-----------------|-----------------|
|                 | V, Min          | V, Max | V, Min          | V, Max | V, Max          | V, Min          | mA              | mA              |
| LVC MOS18       | -0.300          | 0.63   | 1.17            | 1.83   | 0.45            | 1.35            | 4, 8, or 12     | 4, 8, or 12     |

### ➤ SelectIO standard for HDIO Banks : DC Input and Output Levels

| I/O Standard <sup>1, 2</sup> | V <sub>IL</sub> |                              | V <sub>IH</sub>              |                          | V <sub>OL</sub>             | V <sub>OH</sub>             | I <sub>OL</sub> | I <sub>OH</sub> |
|------------------------------|-----------------|------------------------------|------------------------------|--------------------------|-----------------------------|-----------------------------|-----------------|-----------------|
|                              | V, Min          | V, Max                       | V, Min                       | V, Max                   | V, Max                      | V, Min                      | mA              | mA              |
| HSTL_I_18                    | -0.300          | 50% V <sub>CCO</sub> - 0.100 | 50% V <sub>CCO</sub> + 0.100 | V <sub>CCO</sub> + 0.300 | 0.400                       | V <sub>CCO</sub> - 0.400    | 8.0             | -8.0            |
| LVC MOS18                    | -0.300          | 35% V <sub>CCO</sub>         | 65% V <sub>CCO</sub>         | V <sub>CCO</sub> + 0.300 | 0.450                       | V <sub>CCO</sub> - 0.450    | Note 3          | Note 3          |
| LVC MOS25                    | -0.300          | 0.700                        | 1.700                        | V <sub>CCO</sub> + 0.300 | 0.400                       | V <sub>CCO</sub> - 0.400    | Note 3          | Note 3          |
| LVC MOS33                    | -0.300          | 0.800                        | 2.000                        | 3.400                    | 0.400                       | V <sub>CCO</sub> - 0.400    | Note 3          | Note 3          |
| LVTTL                        | -0.300          | 0.800                        | 2.000                        | 3.400                    | 0.400                       | 2.400                       | Note 3          | Note 3          |
| SSTL18_I                     | -0.300          | 50% V <sub>CCO</sub> - 0.125 | 50% V <sub>CCO</sub> + 0.125 | V <sub>CCO</sub> + 0.300 | V <sub>CCO</sub> /2 - 0.470 | V <sub>CCO</sub> /2 + 0.470 | 8.0             | -8.0            |

#### Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *Versal Adaptive SoC SelectIO Resources Architecture Manual (AM010)*.
3. Supported drive strengths of 4, 8, or 12 mA in HDIO banks.

## ➤ SelectIO standard for XPIO Banks : DC Input and Output Levels

| I/O Standard <sup>1, 2, 3</sup> | V <sub>IL</sub> |                              | V <sub>IH</sub>              |                          | V <sub>OL</sub>             | V <sub>OH</sub>             | I <sub>OL</sub> | I <sub>OH</sub> |
|---------------------------------|-----------------|------------------------------|------------------------------|--------------------------|-----------------------------|-----------------------------|-----------------|-----------------|
|                                 | V, Min          | V, Max                       | V, Min                       | V, Max                   | V, Max                      | V, Min                      | mA              | mA              |
| HSTL_I                          | -0.300          | 50% V <sub>CC0</sub> - 0.100 | 50% V <sub>CC0</sub> + 0.100 | V <sub>CC0</sub> + 0.300 | 0.400                       | V <sub>CC0</sub> - 0.400    | 5.8             | -5.8            |
| HSTL_I_12                       | -0.300          | 50% V <sub>CC0</sub> - 0.080 | 50% V <sub>CC0</sub> + 0.080 | V <sub>CC0</sub> + 0.300 | 25% V <sub>CC0</sub>        | 75% V <sub>CC0</sub>        | 4.1             | -4.1            |
| HSUL_12                         | -0.300          | 50% V <sub>CC0</sub> - 0.130 | 50% V <sub>CC0</sub> + 0.130 | V <sub>CC0</sub> + 0.300 | 20% V <sub>CC0</sub>        | 80% V <sub>CC0</sub>        | 0.1             | -0.1            |
| LVC MOS12                       | -0.300          | 35% V <sub>CC0</sub>         | 65% V <sub>CC0</sub>         | V <sub>CC0</sub> + 0.300 | 0.400                       | V <sub>CC0</sub> - 0.400    | Note 4          | Note 4          |
| LVC MOS15                       | -0.300          | 35% V <sub>CC0</sub>         | 65% V <sub>CC0</sub>         | V <sub>CC0</sub> + 0.300 | 0.450                       | V <sub>CC0</sub> - 0.450    | Note 5          | Note 5          |
| LVDCI_15                        | -0.300          | 35% V <sub>CC0</sub>         | 65% V <sub>CC0</sub>         | V <sub>CC0</sub> + 0.300 | 0.450                       | V <sub>CC0</sub> - 0.450    | 7.0             | -7.0            |
| SSTL12                          | -0.300          | 50% V <sub>CC0</sub> - 0.100 | 50% V <sub>CC0</sub> + 0.100 | V <sub>CC0</sub> + 0.300 | V <sub>CC0</sub> /2 - 0.150 | V <sub>CC0</sub> /2 + 0.150 | 8.0             | -8.0            |
| SSTL135                         | -0.300          | 50% V <sub>CC0</sub> - 0.090 | 50% V <sub>CC0</sub> + 0.090 | V <sub>CC0</sub> + 0.300 | V <sub>CC0</sub> /2 - 0.150 | V <sub>CC0</sub> /2 + 0.150 | 9.0             | -9.0            |
| SSTL15                          | -0.300          | 50% V <sub>CC0</sub> - 0.100 | 50% V <sub>CC0</sub> + 0.100 | V <sub>CC0</sub> + 0.300 | V <sub>CC0</sub> /2 - 0.175 | V <sub>CC0</sub> /2 + 0.175 | 10.0            | -10.0           |

### Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *Versal Adaptive SoC SelectIO Resources Architecture Manual (AM010)*.
3. POD10 and POD12 DC input and output levels are shown in Table 11, Table 16, and Table 17.
4. Supported drive strengths of 2, 4, 6, or 8 mA in XPIO banks.
5. Supported drive strengths of 2, 4, 6, 8, or 12 mA in XPIO banks.

## ➤ Complementary Differential SelectIO standard for HDIO Banks : DC Input and Output Levels

| I/O Standard   | V <sub>ICM</sub> (V) <sup>1</sup> |       |       | V <sub>ID</sub> (V) <sup>2</sup> |       | V <sub>OL</sub> (V) <sup>3</sup> | V <sub>OH</sub> (V) <sup>4</sup> | I <sub>OL</sub> | I <sub>OH</sub> |
|----------------|-----------------------------------|-------|-------|----------------------------------|-------|----------------------------------|----------------------------------|-----------------|-----------------|
|                | Min                               | Typ   | Max   | Min                              | Max   | Max                              | Min                              | mA              | mA              |
| DIFF_HSTL_I_18 | 0.300                             | 0.900 | 1.425 | 0.100                            | -     | 0.400                            | V <sub>CC0</sub> - 0.400         | 8.0             | -8.0            |
| DIFF_SSTL18_I  | 0.300                             | 0.900 | 1.425 | 0.100                            | -     | (V <sub>CC0</sub> /2) - 0.47     | (V <sub>CC0</sub> /2) + 0.47     | 8.0             | -8.0            |
| LVDS_25        | 0.300                             | 1.200 | 1.425 | 0.100                            | 0.600 | -                                | -                                | -               | -               |
| SUB_LVDS       | 0.500                             | 0.900 | 1.300 | 0.070                            | -     | -                                | -                                | -               | -               |
| LVPECL         | 0.300                             | 1.200 | 1.425 | 0.100                            | 0.600 | -                                | -                                | -               | -               |
| SLVS_400_25    | 0.070                             | 0.200 | 0.330 | 0.140                            | 0.450 | -                                | -                                | -               | -               |

### Notes:

1. V<sub>ICM</sub> is the input common mode voltage.
2. V<sub>ID</sub> is the input differential voltage (Q -  $\bar{Q}$ ).
3. V<sub>OL</sub> is the single-ended low-output voltage.
4. V<sub>OH</sub> is the single-ended high-output voltage.

## ➤ Complementary Differential SelectIO standard for XPIO Banks : DC Input and Output Levels

| I/O Standard   | V <sub>ICM</sub> (V) <sup>1</sup> |                     |                               | V <sub>ID</sub> (V) <sup>2</sup> |     | V <sub>OL</sub> (V) <sup>3</sup> | V <sub>OH</sub> (V) <sup>4</sup> | I <sub>OL</sub> | I <sub>OH</sub> |
|----------------|-----------------------------------|---------------------|-------------------------------|----------------------------------|-----|----------------------------------|----------------------------------|-----------------|-----------------|
|                | Min                               | Typ                 | Max                           | Min                              | Max | Max                              | Min                              | mA              | mA              |
| DIFF_HSTL_I    | 0.680                             | V <sub>CC0</sub> /2 | (V <sub>CC0</sub> /2) + 0.150 | 0.100                            | -   | 0.400                            | V <sub>CC0</sub> - 0.400         | 5.8             | -5.8            |
| DIFF_HSTL_I_12 | 0.400 x V <sub>CC0</sub>          | V <sub>CC0</sub> /2 | 0.600 x V <sub>CC0</sub>      | 0.100                            | -   | 0.250 x V <sub>CC0</sub>         | 0.750 x V <sub>CC0</sub>         | 4.1             | -4.1            |
| DIFF_HSUL_12   | (V <sub>CC0</sub> /2) - 0.120     | V <sub>CC0</sub> /2 | (V <sub>CC0</sub> /2) + 0.120 | 0.100                            | -   | 20% V <sub>CC0</sub>             | 80% V <sub>CC0</sub>             | 0.1             | -0.1            |
| DIFF_SSTL12    | (V <sub>CC0</sub> /2) - 0.150     | V <sub>CC0</sub> /2 | (V <sub>CC0</sub> /2) + 0.150 | 0.100                            | -   | (V <sub>CC0</sub> /2) - 0.150    | (V <sub>CC0</sub> /2) + 0.150    | 8.0             | -8.0            |
| DIFF_SSTL135   | (V <sub>CC0</sub> /2) - 0.150     | V <sub>CC0</sub> /2 | (V <sub>CC0</sub> /2) + 0.150 | 0.100                            | -   | (V <sub>CC0</sub> /2) - 0.150    | (V <sub>CC0</sub> /2) + 0.150    | 9.0             | -9.0            |
| DIFF_SSTL15    | (V <sub>CC0</sub> /2) - 0.175     | V <sub>CC0</sub> /2 | (V <sub>CC0</sub> /2) + 0.175 | 0.100                            | -   | (V <sub>CC0</sub> /2) - 0.175    | (V <sub>CC0</sub> /2) + 0.175    | 10.0            | -10.0           |

### Notes:

1. V<sub>ICM</sub> is the input common mode voltage.
2. V<sub>ID</sub> is the input differential voltage.
3. V<sub>OL</sub> is the single-ended low-output voltage.
4. V<sub>OH</sub> is the single-ended high-output voltage.

## ➤ Differential SelectIO standard for MIPI\_DPHY : DC Input and Output Levels

| I/O Standard                                      | V <sub>ICM</sub> (V) <sup>1</sup> |     |       | V <sub>ID</sub> (V) <sup>2</sup> |     |     | V <sub>ILHS</sub> <sup>3</sup> | V <sub>IHHS</sub> <sup>3</sup> | V <sub>OCM</sub> (V) <sup>4</sup> |       |       | V <sub>OD</sub> (V) <sup>5</sup> |       |       |
|---------------------------------------------------|-----------------------------------|-----|-------|----------------------------------|-----|-----|--------------------------------|--------------------------------|-----------------------------------|-------|-------|----------------------------------|-------|-------|
|                                                   | Min                               | Typ | Max   | Min                              | Typ | Max | Min                            | Max                            | Min                               | Typ   | Max   | Min                              | Typ   | Max   |
| MIPI_DPHY for operation <1.5 Gb/s <sup>7</sup>    | 0.070                             | –   | 0.330 | 0.070                            | –   | –   | –0.040                         | 0.460                          | 0.150                             | 0.200 | 0.250 | 0.140                            | 0.200 | 0.270 |
| MIPI_DPHY for operation at >1.5 Gb/s <sup>7</sup> | 0.070                             | –   | 0.330 | 0.040                            | –   | –   | –0.040                         | 0.460                          | 0.150                             | 0.200 | 0.250 | 0.140                            | 0.200 | 0.270 |

### Notes:

1. V<sub>ICM</sub> is the input common mode voltage.
2. V<sub>ID</sub> is the input differential voltage (Q –  $\bar{Q}$ ).
3. V<sub>IHHS</sub> and V<sub>ILHS</sub> are the single-ended input high and low voltages, respectively.
4. V<sub>OCM</sub> is the output common mode voltage.
5. V<sub>OD</sub> is the output differential voltage (Q –  $\bar{Q}$ ).
6. LVDS15 is specified in Table 18.
7. High-speed option for MIPI\_DPHY. The V<sub>ID</sub> maximum is aligned with the standard's specification. A higher V<sub>ID</sub> is acceptable as long as the V<sub>IN</sub> specification is also met.

## ➤ GTYP Transceiver : DC Input and Output Levels

### GTYP Transceiver DC Specifications

| Symbol               | DC Parameter                                                               | Conditions                                                        | Min                                              | Typ                        | Max                    | Units |
|----------------------|----------------------------------------------------------------------------|-------------------------------------------------------------------|--------------------------------------------------|----------------------------|------------------------|-------|
| D <sub>VPPIN</sub>   | Differential peak-to-peak input voltage (external AC coupled)              | >10.3125 Gb/s                                                     | 150                                              | –                          | 1250                   | mV    |
|                      |                                                                            | 6.6 Gb/s to 10.3125 Gb/s                                          | 150                                              | –                          | 1250                   | mV    |
|                      |                                                                            | ≤ 6.6 Gb/s                                                        | 150                                              | –                          | 2000                   | mV    |
| V <sub>IN</sub>      | Single-ended input voltage. Voltage measured at the pin referenced to GND. | DC coupled V <sub>GTYP_AVIT</sub> = 1.2V                          | –200                                             | –                          | V <sub>GTYP_AVIT</sub> | mV    |
| V <sub>CMIN</sub>    | Common mode input voltage                                                  | DC coupled V <sub>GTYP_AVIT</sub> = 1.2V                          | –                                                | 2/3 V <sub>GTYP_AVIT</sub> | –                      | mV    |
| D <sub>VPPOUT</sub>  | Differential peak-to-peak output voltage <sup>1</sup>                      | Transmitter output swing is set to 1.1111                         | 800                                              | –                          | –                      | mV    |
| V <sub>CMOUTDC</sub> | Common mode output voltage: DC coupled (equation based) <sup>2</sup>       | When remote RX termination is floating                            | D <sub>VPPOUT</sub> /2                           |                            |                        | mV    |
|                      |                                                                            | When remote RX is terminated to V <sub>RX_TERM</sub> <sup>3</sup> | V <sub>RX_TERM</sub> /2 + D <sub>VPPOUT</sub> /4 |                            |                        | mV    |
| V <sub>CMOUTAC</sub> | Common mode output voltage: AC coupled                                     | Equation based                                                    | D <sub>VPPOUT</sub> /2                           |                            |                        | mV    |
| R <sub>IN</sub>      | Differential input resistance                                              |                                                                   | –                                                | 100                        | –                      | Ω     |
| R <sub>OUT</sub>     | Differential output resistance                                             |                                                                   | –                                                | 100                        | –                      | Ω     |
| T <sub>OSKEW</sub>   | Transmitter output pair (TXP and TXN) intra-pair skew                      |                                                                   | –                                                | –                          | 10                     | ps    |
| C <sub>EXT</sub>     | Recommended external AC coupling capacitor <sup>4</sup>                    |                                                                   | –                                                | 100                        | –                      | nF    |

### Notes:

1. The output swing and pre-emphasis levels are programmable using the GTY and GTYP transceiver attributes discussed in the *Versal Adaptive SoC GTY and GTYP Transceivers Architecture Manual (AM002)* and can result in values lower than reported in this table.
2. Remote RX termination = GND is not supported.
3. V<sub>RX\_TERM</sub> is the remote RX termination voltage. V<sub>CMOUTDC</sub>, V<sub>RX\_TERM</sub> should be less than 0.92V.
4. Other values can be used as appropriate to conform to specific protocols and standards.

## ➤ GTYP Transceiver Clock Output Level Specification

| Symbol | Description                                                 | Conditions                       | Min | Typ | Max | Units |
|--------|-------------------------------------------------------------|----------------------------------|-----|-----|-----|-------|
| VOL    | Output Low voltage for P and N                              | RT = 100Ω across P and N signals | 100 | –   | 330 | mV    |
| VOH    | Output High voltage for P and N                             | RT = 100Ω across P and N signals | 500 | –   | 700 | mV    |
| VDDOUT | Differential output voltage (P–N), P = High (N–P), N = High | RT = 100Ω across P and N signals | 300 | –   | 430 | mV    |
| VCMOUT | Common mode voltage                                         | RT = 100Ω across P and N signals | 300 | –   | 500 | mV    |

## PCB Routing Constrains for Daughter Board

| Signal name                                 | impedance | Max Length | space | Length Matching and note                                                                                                               |
|---------------------------------------------|-----------|------------|-------|----------------------------------------------------------------------------------------------------------------------------------------|
| VCC_CARD_EN<br>LPD_MIO4_GPIO<br>HDIO[0..21] | 50 ohm    | 5"         | 3H *  |                                                                                                                                        |
| GTYP_CLKP/N[0..1]                           | 85 ohm    | 3"         | 5H*   | 1. Difference between P and N traces within a differential pair 0.75ps                                                                 |
| GTYP_TXP/N[0..3]                            | 85 ohm    | 3"         | 5H*   | 1. Difference between P and N traces within a differential pair 0.5ps<br>2. Difference between differential pairs lane to lane <1250ps |
| GTYP_RXP/N[0..3]                            | 85 ohm    | 3"         | 5H*   | 1. Difference between P and N traces within a differential pair 0.5ps<br>2. Difference between differential pairs lane to lane <1250ps |
| XPIO_L[0..26]P/N                            | 100 ohm   | 1.5"       | 5H*   | 1. Difference between P and N traces within a differential pair 0.5ps<br>Note1                                                         |

\* H is the distance to the nearest ground return plane.

Note1: Length Matching Routing Rule for XPIO with different defined

1. For interfacing with PHYs with adjustable internal delays, skew between GEMx\_TX\_DATA[0:3]/GEMx\_TX\_CTRL and GEMx\_TX\_CLK should be within 50 ps.
2. For interfacing with PHYs with adjustable internal delays, skew between GEMx\_RX\_DATA[0:3]/GEMx\_RX\_CTRL and GEMx\_RX\_CLK should be within 50 ps.
3. For interfacing with MIPI. Skew between clock and data should be within  $\pm 2$  ps.

Consult the Versal Adaptive SoC GTYP Transceivers Architecture Manual (AM002) for further details.

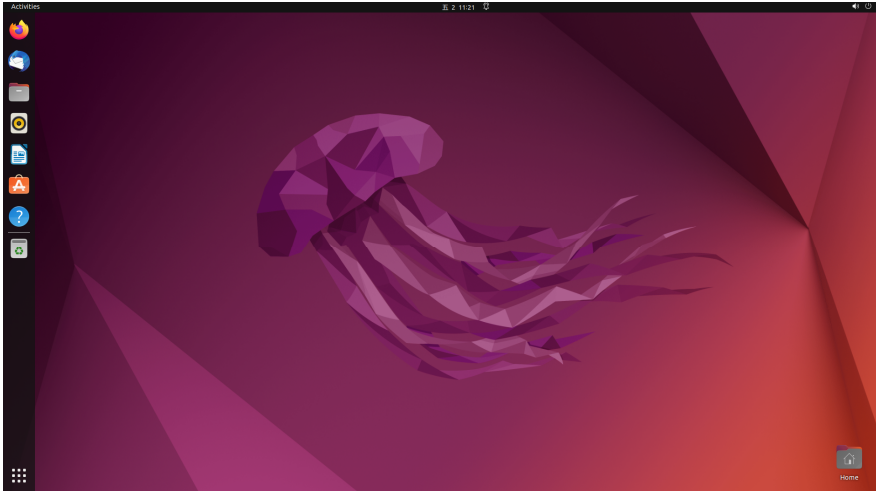
For GTY/GTYP transceiver interfaces such as DisplayPort, SGMII, PCIe®, SATA, and USB3.0, refer to Versal ACAP GTY and GTYP Transceivers Architecture Manual (AM002).  
<https://docs.xilinx.com/r/en-US/am002-versal-gty-transceivers/Transceiver-and-Tool-Overview>

Versal ACAP SelectIO Resources Architecture Manual (AM010)  
<https://docs.xilinx.com/r/en-US/am010-versal-selectio/Overview>

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## **Appendix D: VPR-4616-SYS Default Login**

The VPR-4616-SYS is loaded Ubuntu operating system, after you power on the system, the Ubuntu operating system screen will be appear as shown.



### **Default Login:**

Username: **D773**

Password: **1234**

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